

PAMS Technical Documentation

NSE-3 Series Transceivers

Chapter 3

System Module

CONTENTS

Transceiver NSE-3	3 – 5
Introduction	3 – 5
Functional Description	3 – 5
Interconnection Diagram	3 – 6
System Module	3 – 7
External and Internal Connectors	3 – 7
System Connector Contacts	3 – 8
RF Connector Contacts	3 – 9
Supply Voltages and Power Consumption	3 – 9
Functional Description	3 – 9
Baseband Module	3 – 10
Block Diagram	3 – 10
Technical Summary	3 – 10
Bottom Connector External Contacts	3 – 12
Bottom Connector Signals	3 – 12
Battery Connector	3 – 14
SIM Card Connector	3 – 15
Internal Microphone	3 – 15
Infrared Module Connections	3 – 15
RTC Backup Battery	3 – 16
Buzzer	3 – 16
Functional Description	3 – 17
Power Distribution	3 – 17
Battery charging	3 – 18
Startup Charging	3 – 18
Battery Overvoltage Protection	3 – 19
Battery Removal During Charging	3 – 20
Different PWM Frequencies (1Hz and 32 Hz)	3 – 21
Battery Identification	3 – 22
Battery Temperature	3 – 23
Supply Voltage Regulators	3 – 23
Switched Mode Supply VSIM	3 – 25
Power Up	3 – 25
Power up with a charger	3 – 26
Power Up With The Power Switch (PWRONX)	3 – 26
Power Up by RTC	3 – 27
Power Up by IBI	3 – 27
Acting Dead	3 – 27
Active Mode	3 – 27
Sleep Mode	3 – 27
Charging	3 – 27
Power Off	3 – 28
Watchdog	3 – 28

Audio control	3 – 29
External Audio Connections	3 – 30
Analog Audio Accessory Detection	3 – 31
Headset Detection	3 – 31
Internal Audio Connections	3 – 32
4-wire PCM Serial Interface	3 – 32
Alert Signal Generation	3 – 33
Digital Control	3 – 33
MAD2	3 – 33
Memories	3 – 43
Program Memory	3 – 43
SRAM Memory	3 – 43
EEPROM Memory	3 – 43
MCU Memory Map	3 – 44
Flash Programming	3 – 44
COBBA-GJ	3 – 44
Infrared Transceiver Module	3 – 45
Real Time Clock	3 – 45
RTC backup battery charging	3 – 46
Vibra Alerting Device	3 – 46
IBI Accessories	3 – 47
Phone Power-on by IBI	3 – 47
IBI power-on by phone	3 – 47
RF Module	3 – 48
Maximum Ratings	3 – 48
RF Frequency Plan	3 – 48
Power Distribution Diagram	3 – 49
DC Characteristics	3 – 50
Regulators	3 – 50
Control Signals	3 – 50
Functional Description	3 – 50
Frequency synthesizers	3 – 50
Receiver	3 – 52
Transmitter	3 – 53
AGC strategy	3 – 55
AFC function	3 – 56
Receiver blocks	3 – 56
RX interstage filter	3 – 56
1st mixer in CRFU_1a	3 – 56
1st IF-filter	3 – 56

Transmitter Blocks	3 – 57
TX interstage filter	3 – 57
Power amplifier MMIC	3 – 57
Synthesizer blocks	3 – 57
VHF VCO and low pass filter	3 – 57
UHF PLL	3 – 57
UHF PLL block in PLUSA	3 – 57
UHF VCO module	3 – 58
UHF local signal input in CRFU_1a	3 – 58
Connections	3 – 58
RF connector and antenna switch	3 – 58
Timings	3 – 61
Synthesizer control timing	3 – 61
Transmitter power switching timing diagram	3 – 63
Synthesizer clocking	3 – 63
Block Diagram of Baseband Blocks	3 – 64
Parts list of UP8T (EDMS Issue 11.10)	3 – 65

Schematic Diagrams:

Block Diagram of System/RF Blocks	3/A3-1
Circuit Diagram of Baseband (Version 12 Edit 8)	3/A3-2
Circuit Diagram of Power Supply (Version 14 Edit 41)	3/A3-3
Circuit Diagram of SIM Connectors (Version 14 Edit 9)	3/A3-4
Circuit Diagram of CPU Block (Version 14 Edit 23)	3/A3-5
Circuit Diagram of Audio (Version 14 Edit 27)	3/A3-6
Circuit Diagram of IR Module (Version 14 Edit 21)	3/A3-7
Circuit Diagram of RF Block (Version 14 Edit 26)	3/A3-8
Layout Diagram of UPT8T (Version 14)	3/A3-9

Transceiver NSE-3

Introduction

The NSE-3 is a radio transceiver unit designed for the GSM network. It is a GSM phase 2 power class 4 transceiver providing 15 power levels with a maximum output power of 2 W. The transceiver is a true 3 V transceiver.

The transceiver consists of System/RF module (UP8T), User interface module (UE4) and assembly parts.

The transceiver has full graphic display and two soft key based user interface.

The antenna is a fixed helix. External antenna connection is provided by rear RF connector

Functional Description

There are five different operation modes:

- power off mode
- idle mode
- active mode
- charge mode
- local mode

In the power off mode only the circuits needed for power up are supplied.

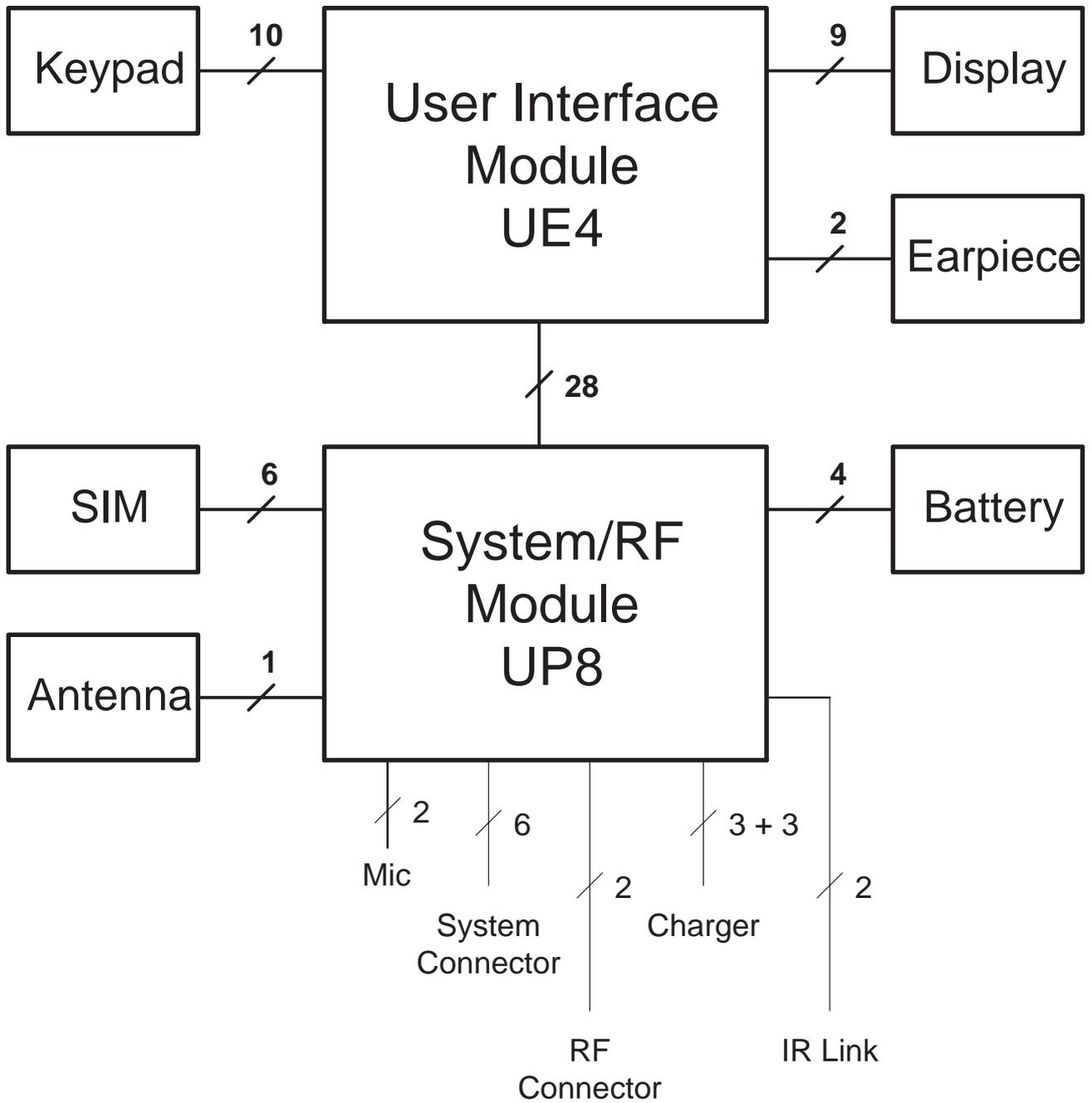
In the idle mode circuits are powered down and only sleep clock is running.

In the active mode all the circuits are supplied with power although some parts might be in the idle state part of the time.

The charge mode is effective in parallel with all previous modes. The charge mode itself consists of two different states, i.e. the charge and the maintenance mode.

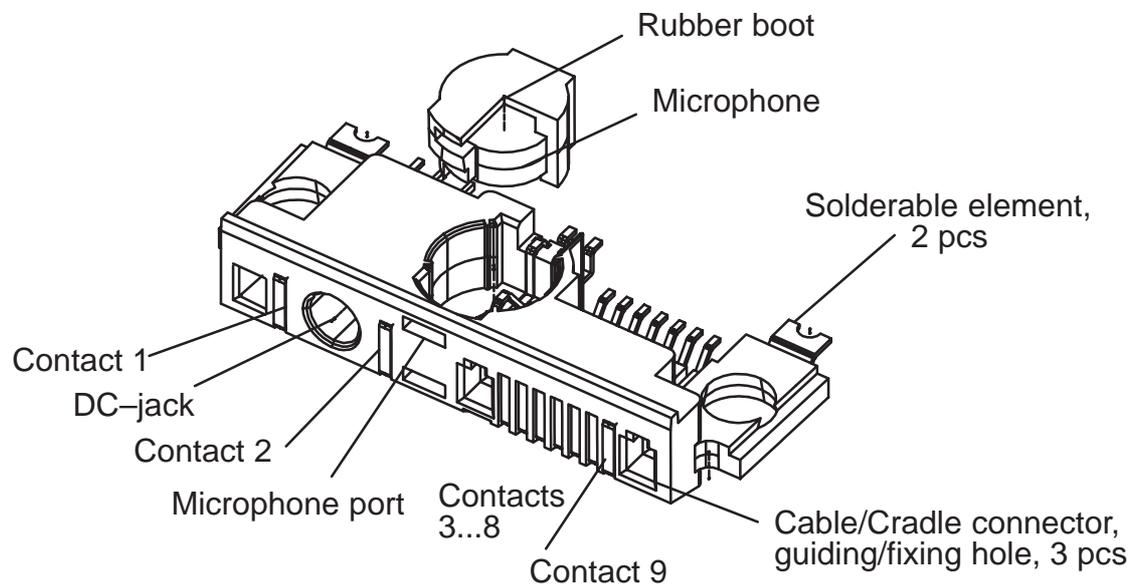
The local mode is used for alignment and testing.

Interconnection Diagram



System Module

External and Internal Connectors



System Connector Contacts

Contact	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	VIN	Charger input voltage Charger input current	7.1 720 7.24 320	8.4 800 7.6 370	9.3 850 16.0 420	V/ Unloaded ACP-9 Charger mA/ Supply current V/ Unloaded ACP-7 Charger mA/ Supply current
DC-JACK	L_GND	Charger ground input	0	0	0	V/ Supply ground
DC-JACK	VIN	Charger input voltage Charger input current	7.1 720 7.24 320	8.4 800 7.6 370	9.3 850 16.0 420	V/ Unloaded ACP-9 Charger mA/ Supply current V/ Unloaded ACP-7 Charger mA/ Supply current
DC-JACK	CHRG CTRL	Output high voltage PWM frequency output low voltage	2.0 0	32	2.8 0.5	V/ Charger control (PWM) high Hz /PWM frequency for charger V
2	CHRG CTRL	Output high voltage PWM frequency	2.0	32	2.8	V/ Charger control (PWM) high Hz /PWM frequency for charger
Mic ports		Acoustic signal	N/A	N/A	N/A	Microphone sound ports
3	XMIC	Input signal voltage		60	1 Vpp	mVrms
4	SGND	Signal ground	0		0	mVrms
5	XEAR	Output signal voltage		80	1 Vpp	mVrms
6	MBUS	I/O low voltage I/O high voltage	0 2.0		0.8 2.8	Serial bidirectional control bus. Baud rate 9600 Bit/s
7	FBUS_RX	Input low voltage Input high voltage	0 2.0		0.8 2.8	V/ Fbus receive. V/ Serial Data, Baud rate 9.6k-230.4kBit/s
8	FBUS_TX	Output low voltage Output high voltage	0 2.0		0.8 2.8	V/ Fbus transmit. V/ Serial Data, Baud rate 9.6k-230.4kBit/s
9	L_GND	Charger ground input	0	0	0	V/ Supply ground

RF Connector Contacts

Contact	Line Symbol	Parameter	Minimum	Typical / Nominal	Maximum	Unit / Notes
1	EXT_ANT	Impedance		50ohm		External antenna connector, 0 V DC
2	GND					

Supply Voltages and Power Consumption

Connector	Line Symbol	Minimum	Typical / Nominal	Maximum/ Peak	Unit / Notes
Charging	VIN	7.1	8.4	9.3	V/ Travel charger, ACP-9
Charging	VIN	7.25	7.6	16.0	V/ Travel charger, ACP-7
Charging	I / VIN	720	800	850	mA/ Travel charger, ACP-9
Charging	I / VIN	320	370	420	mA/ Travel charger, ACP-7

Functional Description

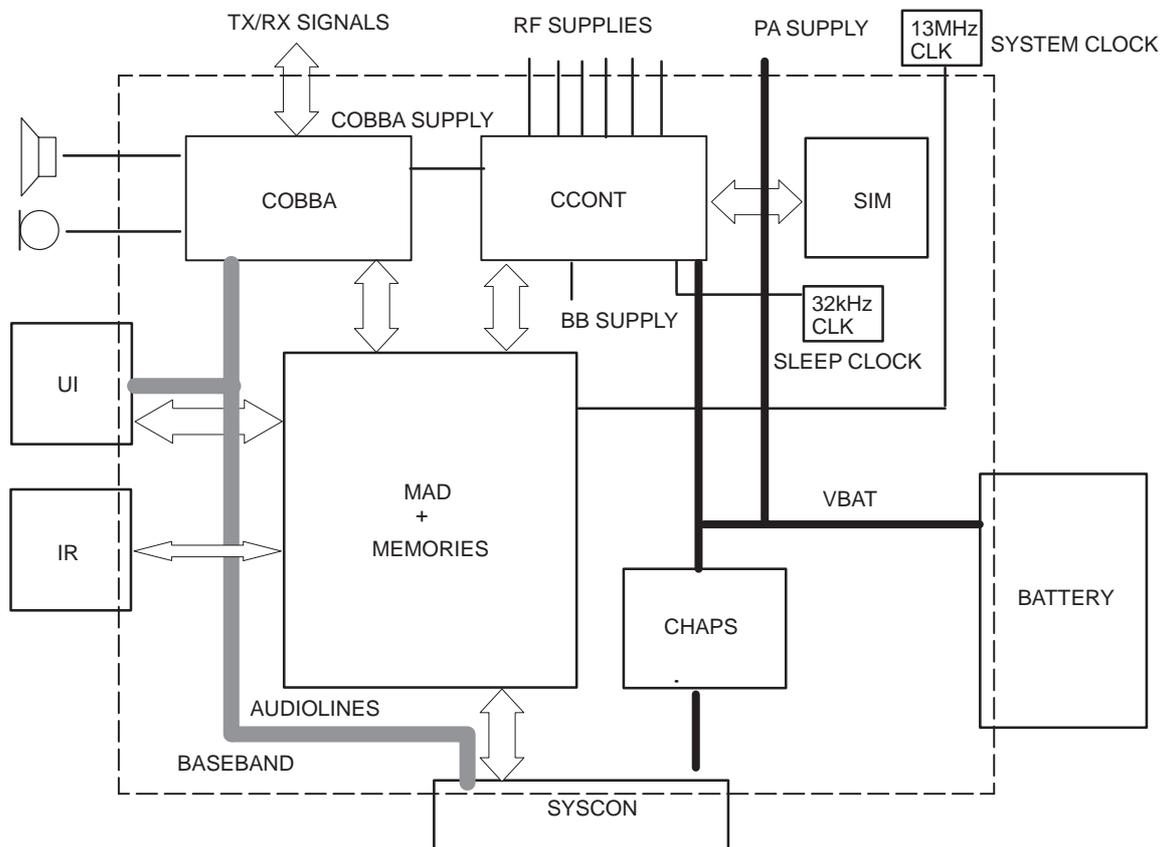
The transceiver electronics consist of the Radio Module ie. RF + System blocks, the UI PCB, the display module and audio components. The keypad and the display module are connected to the Radio Module with a connectors. System blocks and RF blocks are interconnected with PCB wiring. The Transceiver is connected to accessories via a bottom system connector with charging and accessory control.

The System blocks provide the MCU, DSP and Logic control functions in MAD ASIC, external memories, audio processing and RF control hardware in COBBA ASIC. Power supply circuitry CCONT ASIC delivers operating voltages both for the System and the RF blocks.

The RF block is designed for a handportable phone which operates in the GSM system. The purpose of the RF block is to receive and demodulate the radio frequency signal from the base station and to transmit a modulated RF signal to the base station. The PLUSSA ASIC is used for VHF and PLL functions. The CRFU ASIC is used at the front end.

Baseband Module

Block Diagram



Technical Summary

The baseband module consists of four asics, CHAPS, CCONT, COBBA-GJ and MAD2, which take care of the baseband functions of NSE-3.

The baseband is running from a 2.8V power rail, which is supplied by a power controlling asic. In the CCONT asic there are 6 individually controlled regulator outputs for RF-section and two outputs for the baseband. In addition there is one +5V power supply output (V5V) for flash programming voltage and other purposes where a higher voltage is needed. The CCONT contains also a SIM interface, which supports both 3V and 5V SIM-cards. A real time clock function is integrated into the CCONT, which utilizes the same 32kHz clock supply as the sleep clock. A backup power supply is provided for the RTC, which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargeable polyacene battery. The backup time with this battery is minimum of ten minutes.

The interface between the baseband and the RF section is handled by a specific asic. The COBBA asic provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the UI section. The COBBA supplies the analog TXC and AFC signals to rf section according to the MAD DSP digital control and converts analog AGC into digital signal for the DSP. Data transmission between the COBBA and the MAD is implemented using a parallel connection for high speed signalling and a serial connection for PCM coded audio signals. Digital speech processing is handled by the MAD asic. The COBBA asic is a dual voltage circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA.

The baseband supports three external microphone inputs and two external earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA asic.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. Input and output signal source selection and gain control is performed inside the COBBA asic according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding. A buzzer and an external vibra alert control signals are generated by the MAD with separate PWM outputs.

EMC shielding is implemented using a metallized plastic B-cover with a conductive rubber seal on the ribs. On the other side the engine is shielded with a frame having a conductive rubber on the inner walls, which makes a contact to a ground ring of the engine board and a ground plane of the UI-board. Heat generated by the circuitry will be conducted out via the PCB ground planes.

Bottom Connector External Contacts

Contact	Line Symbol	Function
1	VIN	Charger input voltage
DC-jack side contact (DC-plug ring)	L_GND	Charger ground
DC-jack center pin	VIN	Charger input voltage
DC-jack side contact (DC-plug jacket)	CHRG_CTRL	Charger control output (from phone)
2	CHRG_CTRL	Charger control output (from phone)
Microphone acoustic ports		Acoustic signal (to phone)
3	XMIC	Accessory microphone signal input (to phone)
4	SGND	Accessory signal ground
5	XEAR	Accessory earphone signal output (from phone)
6	MBUS	MBUS, bidirectional serial data i/o
7	FBUS_RX	FBUS, unidirectional serial data input (to phone)
8	FBUS_TX	FBUS, unidirectional serial data output (from phone)
9	L_GND	Charger ground

Bottom Connector Signals

Pin	Name	Min	Typ	Max	Unit	Notes
1,3	VIN	7.25	7.6	7.95	V	Unloaded ACP-7 Charger (5kohms load)
				16.9	V	
		3.25	3.6	3.95	V	Peak output voltage (5kohms load)
		320	370	420	mA	Loaded output voltage (10ohms load) Supply current
		7.1	8.4	9.3	V	Unloaded ACP-9 Charger
		3.25	3.6	3.95	V	Loaded output voltage (10ohms load)
		720	800	850	mA	Supply current
2	L_GND	0		0	V	Supply ground
4,5	CHRG_CTRL	0		0.5	V	Charger control PWM low
		2.0		2.85	V	Charger control PWM high
			32		Hz	PWM frequency for a fast charger
		1		99	%	PWM duty cycle
6	MICP		N/A			see section Internal microphone
7	MICN		N/A			see section Internal microphone

Pin	Name	Min	Typ	Max	Unit	Notes
8	XMIC	2.0		2.2	k Ω	Input AC impedance
				1	V _{pp}	Maximum signal level
		1.47		1.55	V	Mute (output DC level)
		2.5		2.85	V	Unmute (output DC level)
		100		600	μ A	Bias current
		58		490	mV	Maximum signal level
	HMIC	0	3.2	29.3	mV	Microphone signal Connected to COBBA MIC3P input
9	SGND		47		Ω	Output AC impedance (ref. GND)
			10		μ F	Series output capacitance
			380		Ω	Resistance to phone ground
10	XEAR		47		Ω	Output AC impedance (ref. GND)
			10		μ F	Series output capacitance
		16		300	Ω	Load AC impedance to SGND (Headset)
		4.7	10		k Ω	Load AC impedance to SGND (Accessory)
			1.0		V _{pp}	Maximum output level (no load)
			22	626	mV	Output signal level
			10		k Ω	Load DC resistance to SGND (Accessory)
		16		1500	Ω	Load DC resistance to SGND (Headset)
		2.8		V	DC voltage (47k pull-up to VBB)	
	HEAR		28	626	mV	Earphone signal (HF- HFCM) Connected to COBBA HF output
11	MBUS	0 2.0	logic low logic high	0.8 2.85	V	Serial bidirectional control bus. Baud rate 9600 Bit/s Phone has a 4k7 pullup resistor
12	FBUS_RX	0 2.0	logic low logic high	0.8 2.85	V	Fbus receive. Serial Data Baud rate 9.6k–230.4kBit/s Phone has a 220k pulldown resistor
13	FBUS_TX	0 2.0	logic low logic high	0.5 2.85	V	Fbus transmit. Serial Data Baud rate 9.6k–230.4kBit/s Phone has a 47k pullup resistor
14	GND	0		0.3	V	Supply ground

Battery Connector

Pin	Name	Min	Typ	Max	Unit	Notes
1	BVOLT	3.0	3.6	4.5 5.0 5.3	V	Battery voltage Maximum voltage in call state with charger Maximum voltage in idle state with charger
2	BSI	0		2.85	V	Battery size indication Phone has 100kohm pull up resistor. SIM Card removal detection (Treshold is 2.4V@VBB=2.8V)
		2.2		18	kohm	Battery indication resistor (Ni battery)
		20	22	24	kohm	Battery indication resistor (service battery)
		27		51	kohm	Battery indication resistor (4.1V Lithium battery)
		68		91	kohm	Battery indication resistor (4.2V Lithium battery)
3	BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+-5%) pullup resistor, Battery package has a NTC pulldown resistor: 47k+-5%@+25C , B=4050+-3%
		2.1		3	V	Phone power up by battery (input)
		5	10	20	ms	Power up pulse width
		1.9		2.85	V	Battery power up by phone (output)
		90	100	200	ms	Power up pulse width
0		1	kohm	Local mode initialization (in production)		
20	22	25	kHz	PWM control to VIBRA BATTERY		
4	BGND	0		0	V	Battery ground

SIM Card Connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
4	GND	GND	0		0	V	Ground
3, 5	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	"1" "0" "1" "0"	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us
2	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	"1" "1"	VSIM VSIM	V	SIM reset
1	SIMCLK	Frequency Trise/Tfall		3.25		MHz ns	SIM clock

Internal Microphone

Pin	Name	Min	Typ	Max	Unit	Notes
6	MICP		0.55	4.1	mV	Connected to COBBA MIC2N input. The maximum value corresponds to 1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB. typical value is maximum value – 16 dB.
7	MICN		0.55	4.1	mV	Connected to COBBA MIC2P input. The maximum value corresponds to 1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB. typical value is maximum value – 16 dB.

Infrared Module Connections

An infrared transceiver module is designed to substitute an electrical cable between the phone and a PC. The infrared transceiver module is a stand alone component capable to perform infrared transmitting and receiving functions by transforming signals transmitted in infrared light from and to electrical data pulses running in two wire asynchronous databus. In DCT3 the module is placed inside the phone at the top of the phone.

Signal	Parameter	Min	Typ	Max	Unit	Notes
IRON	IR-module on/off	2.0		2.85	V	Iout@2mA
FBUS_RX	IR receive pulse	0		0.8	V	
	IR receive no pulse	2.0		2.85	V	
FBUS_TX	IR transmit pulse	2.0		2.85	V	Iout@2mA
	IR transmit no pulse	0		0.5	V	

RTC Backup Battery

The RTC block in CCONT needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargeable polyacene battery that can keep the clock running minimum of 10 minutes. The backup battery is charged from the main battery through CHAPS.

Signal	Parameter	Min	Typ	Max	Unit	Notes
VBACK	Backup battery charging from CHAPS	3.02	3.15	3.28	V	
	Backup battery charging from CHAPS	100	200	500	uA	Vout@VBAT-0.2V
VBACK	Backup battery supply to CCONT	2		3.28	V	Battery capacity 65uAh
	Backup battery supply to CCONT		80		uA	

Buzzer

Signal	Maximum output current	Input high level	Input low level	Level (PWM) range, %	Frequency range, Hz
BuzzPWM / BUZZER	2mA	2.5V	0.2V	0...50 (128 linear steps)	440...4700

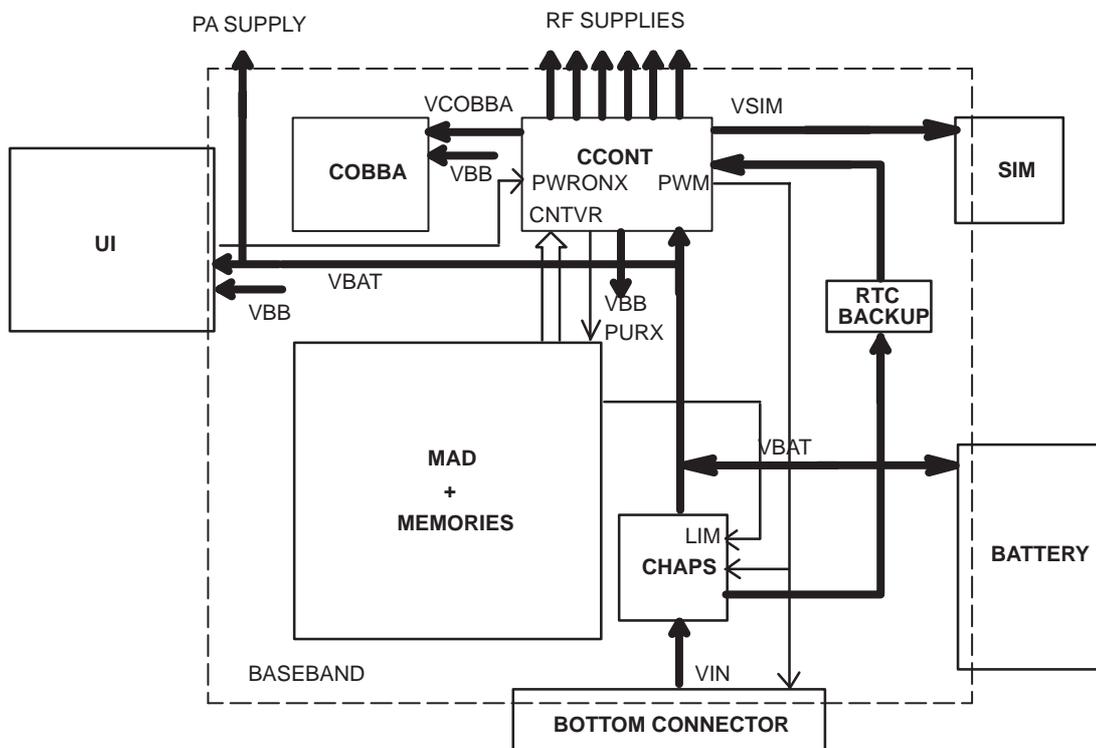
Functional Description

Power Distribution

In normal operation the baseband is powered from the phone's battery. The battery consists of one Lithium-Ion cell. There is also a possibility to use batteries consisting of three Nickel Metal Hydride cells. An external charger can be used for recharging the battery and supplying power to the phone. The charger can be either a standard charger that can deliver around 400 mA or so called performance charger, which can deliver supply current up to 850 mA.

The baseband contains components that control power distribution to whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to three parts of the system: CCONT, power amplifier, and UI (buzzer and display and keyboard lights). Figure 4 shows a block diagram of the power distribution.

The power management circuit CHAPS provides protection against over-voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.



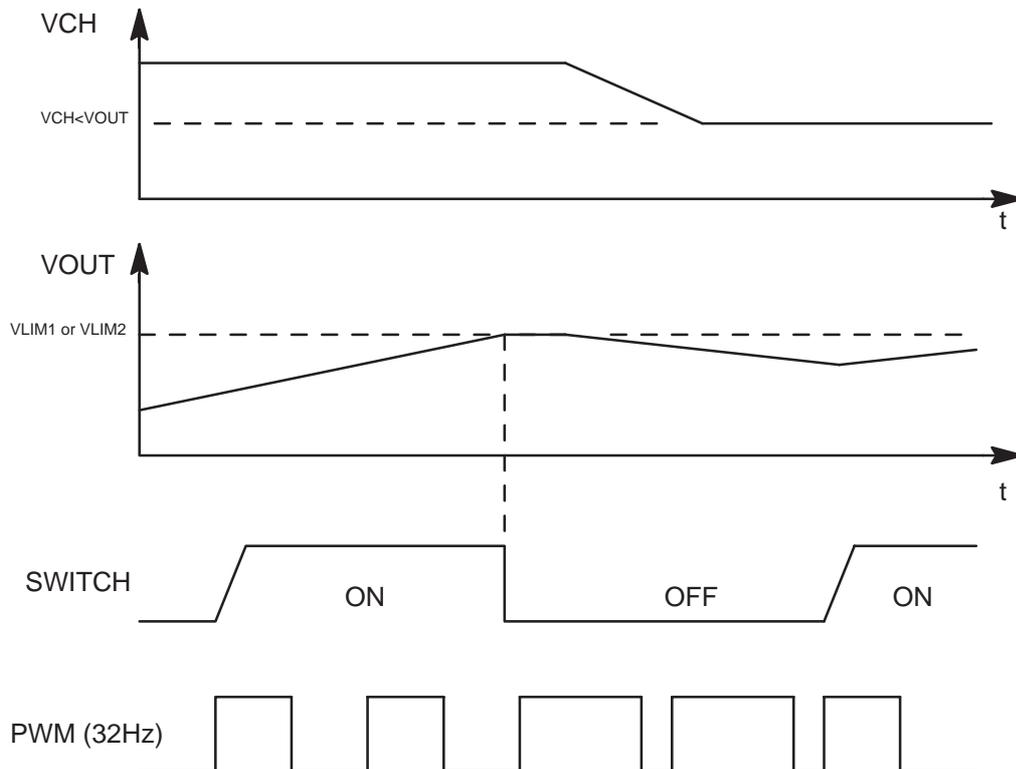
Battery Overvoltage Protection

Output overvoltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni). The power switch is immediately turned OFF if the voltage in VOUT rises above the selected limit VLIM1 or VLIM2.

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM1	LOW	4.4	4.6	4.8	V
Output voltage cutoff limit (no transmission or Ni-battery)	VLIM2	HIGH	4.8	5.0	5.2	V

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N101) LIM- input pin. Default value is lower limit VLIM1.

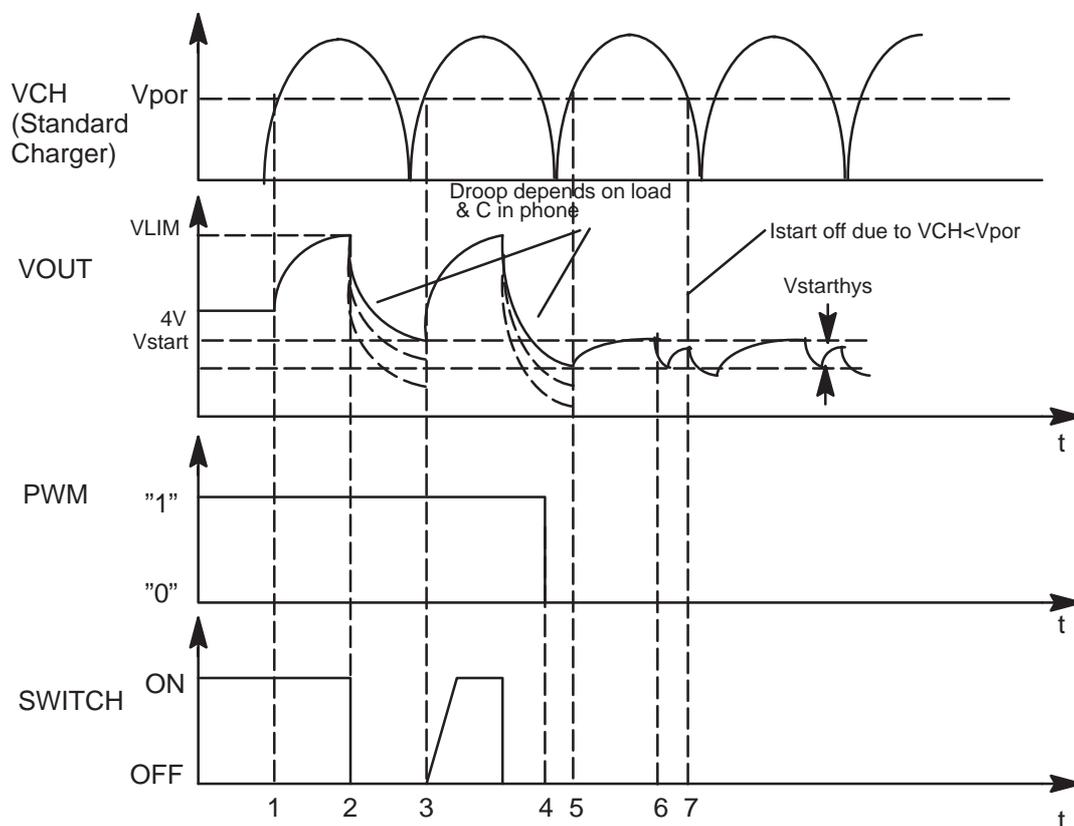
When the switch in output overvoltage situation has once turned OFF, it stays OFF until the the battery voltage falls below VLIM1 (or VLIM2) and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.



Battery Removal During Charging

Output overvoltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM1 (or VLIM2), CHAPS turns switch OFF until the charger input has sunken below Vpor (nominal 3.0V, maximum 3.4V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed. The CHAPS remains in protection state as long as PWM stays HIGH after the output overvoltage situation has occurred.

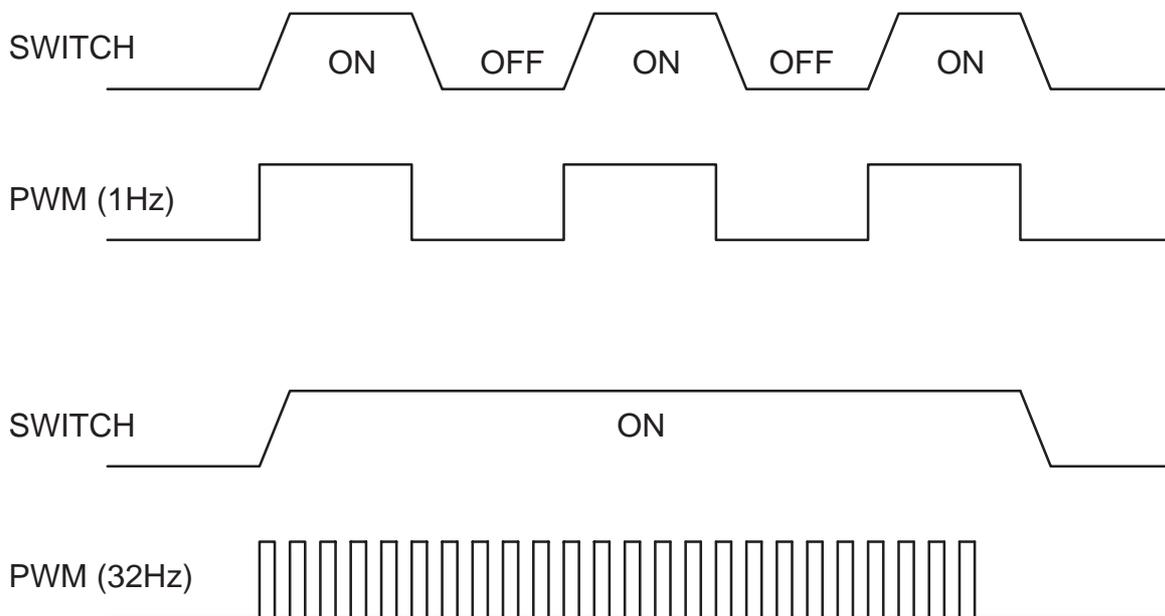


1. Battery removed, (standard) charger connected, VOUT rises (follows charger voltage)
2. VOUT exceeds limit VLIM(X), switch is turned immediately OFF
3. VOUT falls (because no battery), also $V_{CH} < V_{por}$ (standard chargers full-rectified output). When $V_{CH} > V_{por}$ and $V_{OUT} < VLIM(X)$ → switch turned on again (also PWM is still HIGH) and VOUT again exceeds VLIM(X).
4. Software sets PWM = LOW → CHAPS does not enter PWM mode
5. PWM low → Startup mode, startup current flows until Vstart limit reached
6. VOUT exceeds limit Vstart, Istart is turned off
7. VCH falls below Vpor

Different PWM Frequencies (1Hz and 32 Hz)

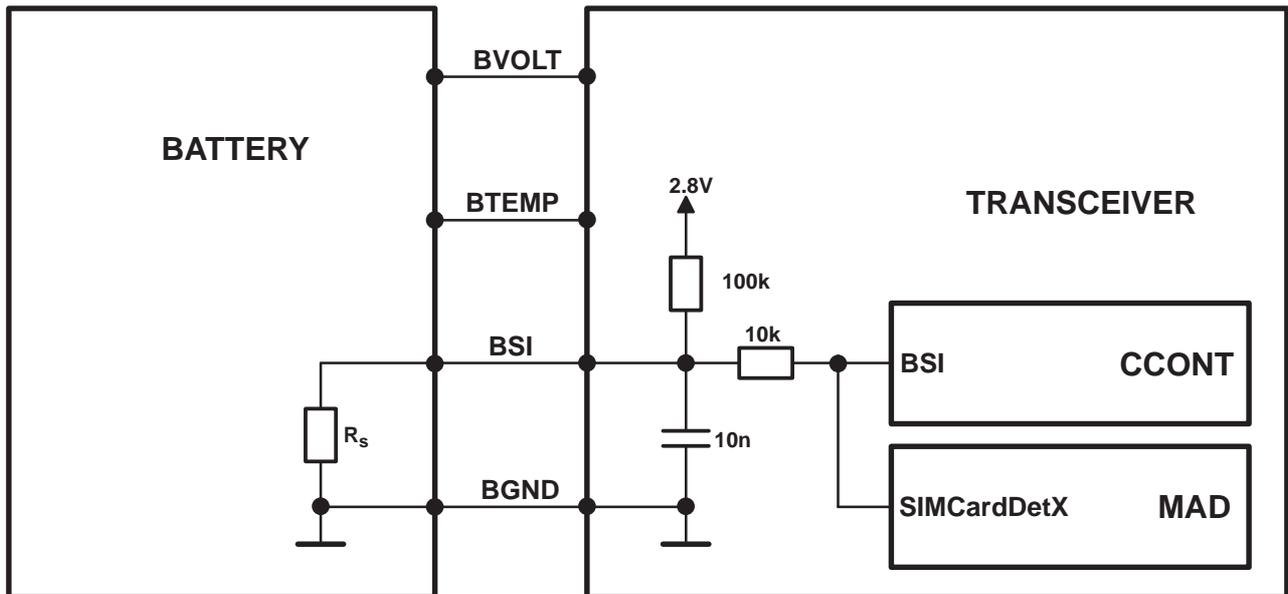
When a travel charger (2– wire charger) is used, the power switch is turned ON and OFF by the PWM input when the PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current $I_{out} = I_{charger} - I_{CHAPS}$ supply current. When PWM is LOW, the switch is OFF and the output current $I_{out} = 0$. To prevent the switching transients inducing noise in audio circuitry of the phone soft switching is used.

The performance travel charger (3– wire charger) is controlled with PWM at a frequency of 32Hz. When the PWM rate is 32Hz CHAPS keeps the power switch continuously in the ON state.

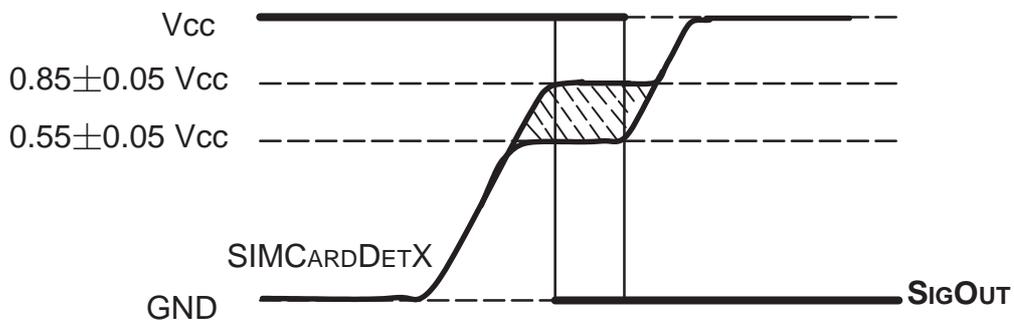


Battery Identification

Different battery types are identified by a pulldown resistor inside the battery pack. The BSI line inside transceiver has a 100k pullup to VBB. The MCU can identify the battery by reading the BSI line DC-voltage level with a CCONT (N100) A/D-converter.

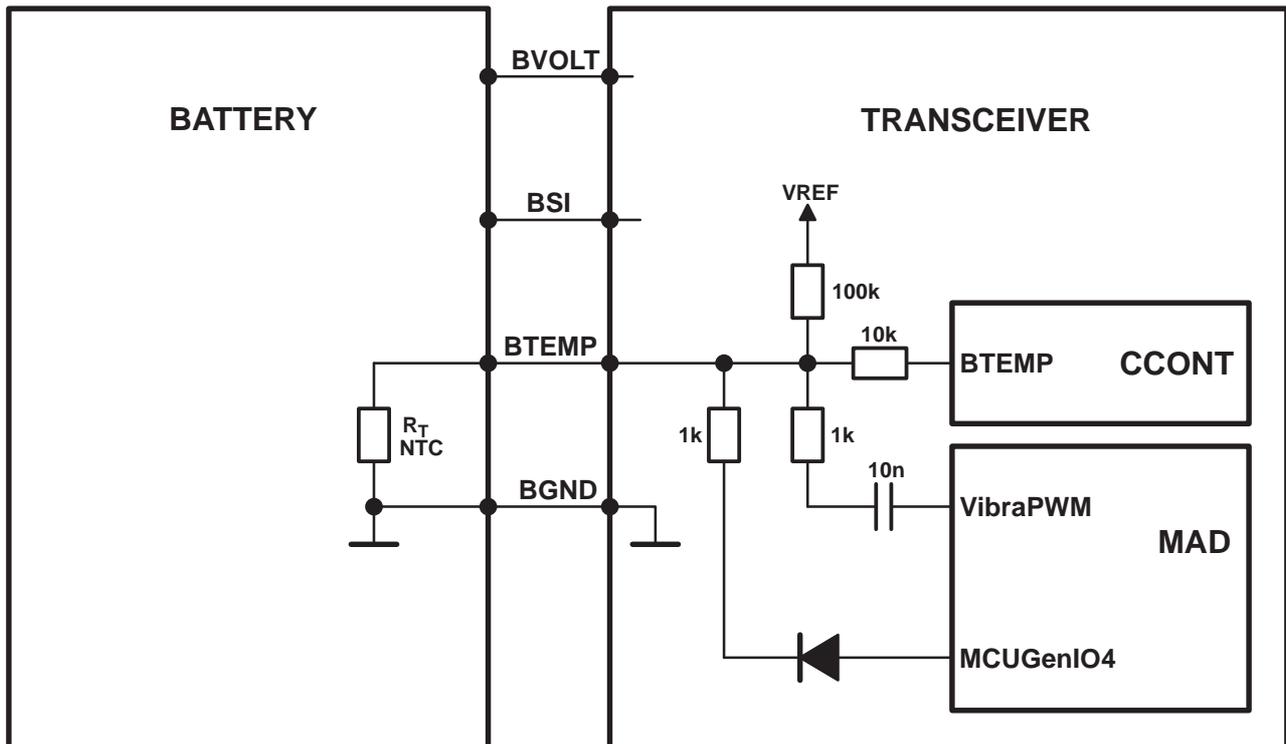


The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2 (D200). SIMCardDetX is a threshold detector with a nominal input switching level $0.85 \times V_{cc}$ for a rising edge and $0.55 \times V_{cc}$ for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery pack is made 0.7mm shorter than the supply voltage contacts so that there is a delay between battery removal detection and supply power off,



Battery Temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pullup to VREF. The MCU can calculate the battery temperature by reading the BTEMP line DC-voltage level with a CCONT (N100) A/D-converter.



Supply Voltage Regulators

The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for a SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF and for flash VPP. The CCONT contains a real time clock function, which is powered from a RTC backup when the main battery is disconnected.

The RTC backup is rechargeable polyacene battery, which has a capacity of 50uAh (@3V/2V) The battery is charged from the main battery voltage by the CHAPS when the main battery voltage is over 3.2V. The charging current is 200uA (nominal).

Operating mode	Vref	RF REG	VCOB-BA	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On/Off
Reset	On	Off VR1 On	On	On	Off	Pull down
Sleep	On	Off	On	On	On	On/Off

NOTE:

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are the listed the MAD control lines and the regulators they are controlling.

- TxPwr controls VTX regulator (VR5)
- RxPwr controls VRX regulator (VR2)
- SynthPwr controls VSYN_1 and VSYN_2 regulators (VR4 and VR3)
- VCXOPwr controls VXO regulator (VR1)

CCONT generates also a 1.5 V reference voltage VREF to COBBA, PLUSSA and CRFU. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

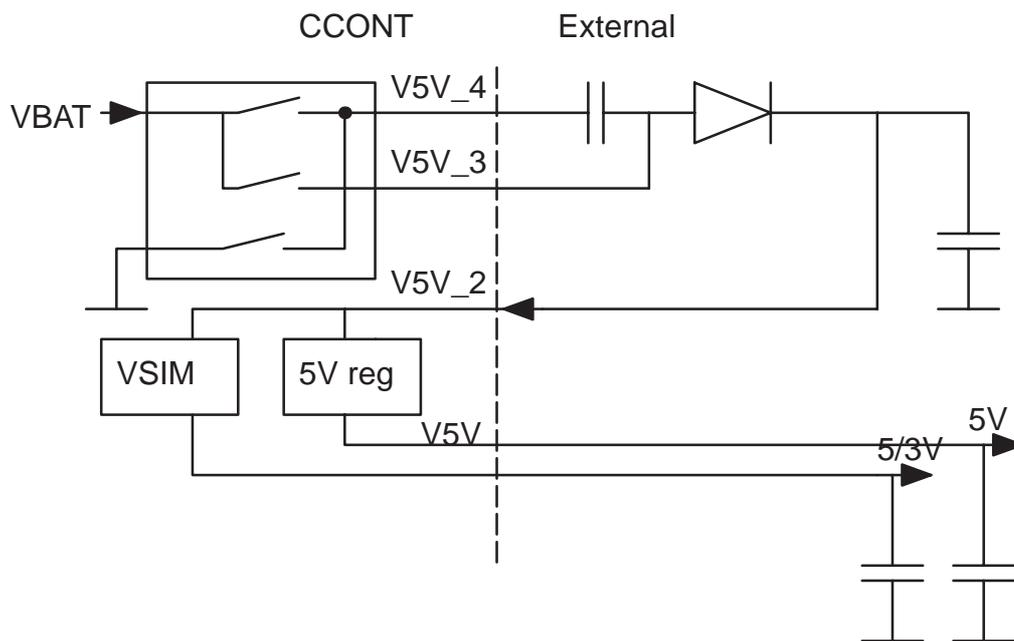
In addition to the above mentioned signals MAD includes also TXP control signal which goes to PLUSSA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA to PLUSSA.

Switched Mode Supply VSIM

There is a switched mode supply for SIM-interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

NOTE: VSIM and V5V can give together a total of 30mA.

In the next figure the principle of the SMR / VSIM-functions is shown.



Power Up

The baseband is powered up by:

6. Pressing the power key, that generates a PWRONX interrupt signal from the power key to the CCONT, which starts the power up procedure.
7. Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.
8. A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power on signal to the CCONT just like the power key.
9. A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

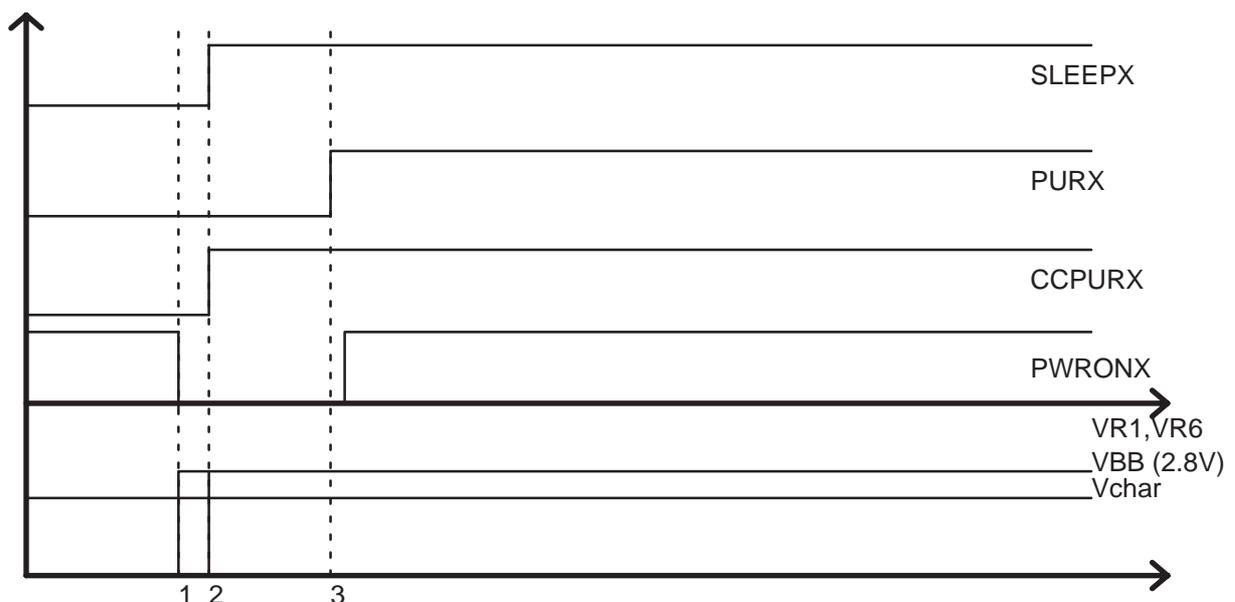
Power up with a charger

When the charger is connected CCONT will switch on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay MAD reset is released, and VCXO –control (SLEEPX) is given to MAD. The diagram assumes empty battery, but the situation would be the same with full battery:

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard powerup procedure and the powerup must be delayed.

Power Up With The Power Switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO as was the case with the charger driven power up. If PWRONX is low when the 64 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 64 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts)



- 1:Power switch pressed ==> Digital voltages on in CCONT (VBB)
- 2: CCONT digital reset released. VCXO turned on
- 3: 62 ms delay to see if power switch is still pressed.

Power Up by RTC

RTC (internal in CCONT) can power the phone up by changing RTCPwr to logical "1". RTCPwr is an internal signal from the CCONT digital section.

Power Up by IBI

IBI can power CCONT up by sending a short pulse to logical "1". RTCPwr is an internal signal from the CCONT digital section.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called "acting dead". To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several substates in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc..

Sleep Mode

In the sleep mode, all the regulators except the baseband VBB, VCOBBA, and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnect during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging can be performed in any operating mode. The charging algorithm is dependent on the used battery technology. The battery type is in-

icated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

The battery voltage, temperature, size and current are measured by the CCONT controlled by the charging software running in the MAD.

The power management circuitry controls the charging current delivered from the charger to the battery. Charging is controlled with a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached 4.2V (Lilon) or 5.2V (NiMH, 5V in call mode). Charging current is monitored by measuring the voltage drop across a 220mohm resistor.

Power Off

The baseband is powered down by:

1. Pressing the power key, that is monitored by the MAD, which starts the power down procedure.
2. If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.
3. Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.
4. Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT just like the power key.

The power down is controlled by the MAD. When the power key has been pressed long enough or the battery voltage is dropped below the limit the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

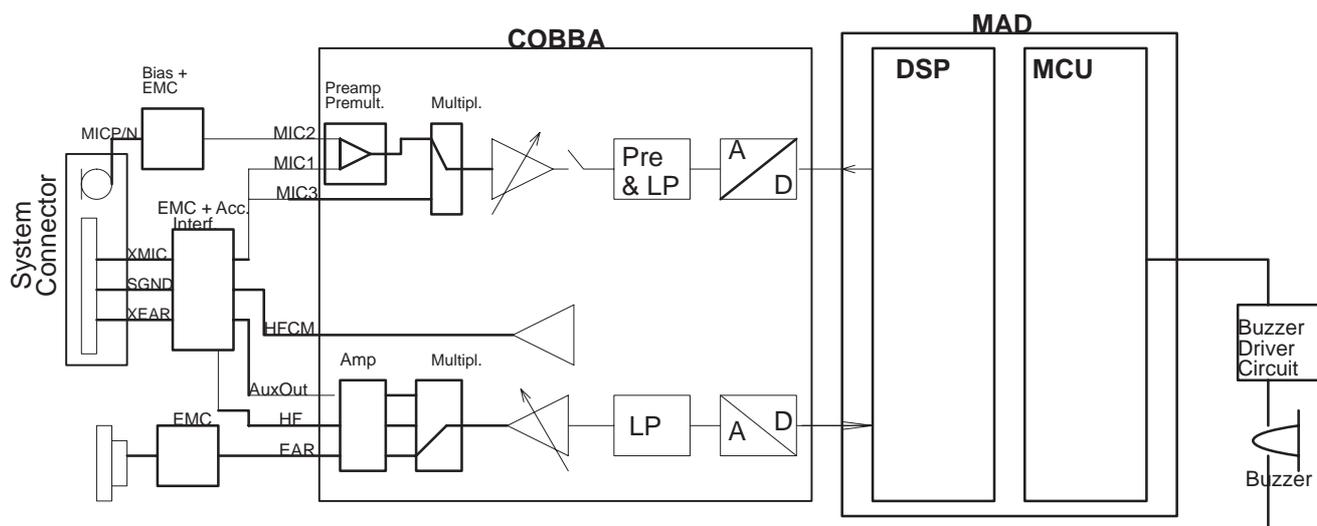
If a charger is connected when the power key is pressed the phone enters into the acting dead mode.

Watchdog

The Watchdog block inside CCONT contains a watchdog counter and some additional logic which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low. The WD-counter runs during that time, though. Watchdog counter is reset internally to 32s at power up. Normally it is reset by MAD writing a control word to the WReg.

Audio control

The audio control and processing is taken care by the COBBA-GJ, which contains the audio and RF codecs, and the MAD2, which contains the MCU, ASIC and DSP blocks handling and processing the audio signals. A detailed audio specification can be found from document



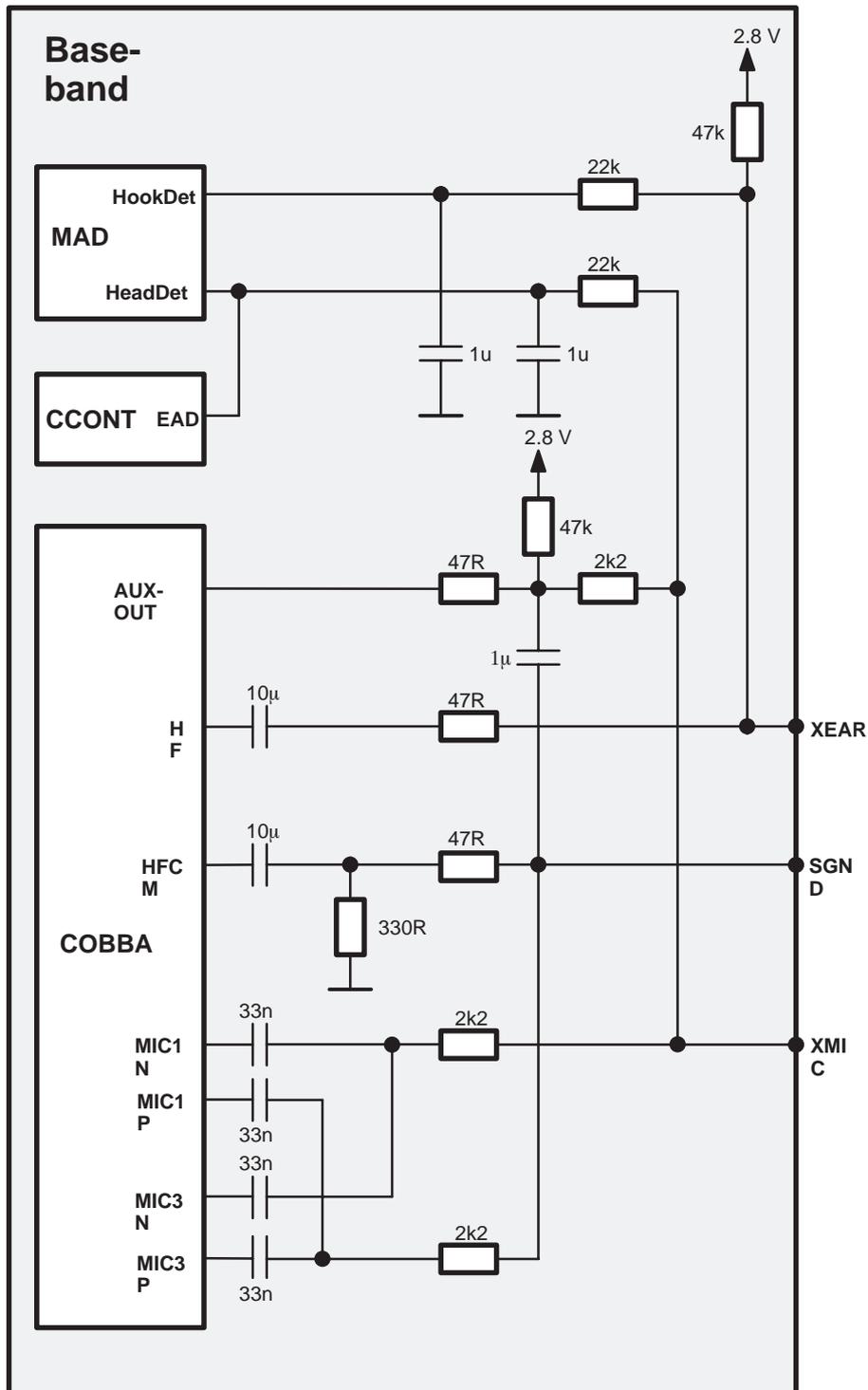
The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA-GJ asic. Inputs for the microphone signals are differential type.

The MIC1 inputs are used for a headset microphone that can be connected directly to the system connector. The internal microphone is connected to MIC2 inputs and an external pre-amplified microphone (handset/handfree) signal is connected to the MIC3 inputs. In COBBA there are also three audio signal outputs of which dual ended EAR lines are used for internal earpiece and HF line for accessory audio output. The third audio output AUXOUT is used only for bias supply to the headset microphone. As a difference to DCT2 generation the SGND (= HFCM at COBBA) does not supply audio signal (only common mode). Therefore there are no electrical loopback echo from downlink to uplink.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. The output for the external accessory and the headset is single ended with a dedicated signal ground SGND. Input and output signal source selection and gain control is performed inside the COBBA-GJ asic according to control messages from the MAD2. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD2 and transmitted to the COBBA-GJ for decoding.

External Audio Connections

The external audio connections are presented in figure 16. A headset can be connected directly to the system connector. The headset microphone bias is supplied from COBBA AUXOUT output and fed to microphone through XMIC line. The 330ohm resistor from SGND line to AGND provides a return path for the bias current.



Analog Audio Accessory Detection

In XEAR signal there is a 47 k Ω pullup in the transceiver and 6.8 k Ω pull-down to SGND in accessory. The XEAR is pulled down when an accessory is connected, and pulled up when disconnected. The XEAR is connected to the HookDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between XEAR and HookDet to prevent audio signal giving unwanted interrupts.

External accessory notices powered-up phone by detecting voltage in XMIC line. In Table 23 there is a truth table for detection signals.

Accessory connected	HookDet	HeadDet	Notes
No accessory connected	High	High	Pullups in the transceiver
Headset HDC-9 with a button switch pressed	Low	Low	XEAR and XMIC loaded (dc)
Headset HDC-9 with a button switch released	High	Low *)	XEAR unloaded (dc)
Handsfree (HFU-1)	Low	High	XEAR loaded (dc)

Headset Detection

The external headset device is connected to the system connector, from which the signals are routed to COBBA headset microphone inputs and earphone outputs. In the XMIC line there is a (47 + 2.2) k Ω pullup in the transceiver. The microphone is a low resistance pulldown compared to the transceiver pullup.

When there is no call going, the AUXOUT is in high impedance state and the XMIC is pulled up. When a headset is connected, the XMIC is pulled down. The XMIC is connected to the HeadDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between the XMIC and the HeadDet to prevent audio signal giving unwanted interrupts (when an accessory is connected).

In the XEAR line there is a 47 k Ω pullup in the transceiver. The earphone is a low resistance pulldown compared to the transceiver pullup. When a remote control switch is open, there is a capacitor in series with the earphone, so the XEAR (and HookDet) is pulled up by the phone. When the switch is closed, the XEAR (and HookDet) is pulled down via the earphone. So both press and release of the button gives an interrupt.

During a call there is a bias voltage (1.5 V) in the AUXOUT, and the HeadDet cannot be used. The headset interrupts should to be disabled during a call and the EAD line (AD converter in CCONT) should be polled to see if the headset is disconnected.

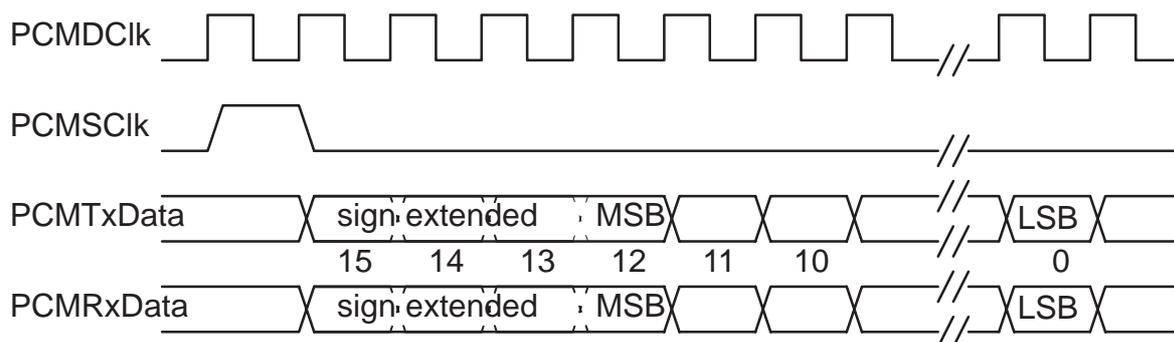
Internal Audio Connections

The speech coding functions are performed by the DSP in the MAD2 and the coded speech blocks are transferred to the COBBA-GJ for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA-GJ by the DSP.

There are two separate interfaces between MAD2 and COBBA-GJ: a parallel bus and a serial bus. The parallel bus has 12 data bits, 4 address bits, read and write strobes and a data available strobe. The parallel interface is used to transfer all the COBBA-GJ control information (both the RFI part and the audio part) and the transmit and receive samples. The serial interface between MAD2 and COBBA-GJ includes transmit and receive data, clock and frame synchronisation signals. It is used to transfer the PCM samples. The frame synchronisation frequency is 8 kHz which indicates the rate of the PCM samples and the clock frequency is 1 MHz. COBBA is generating both clocks.

4-wire PCM Serial Interface

The interface consists of following signals: a PCM codec master clock (PCMDClk), a frame synchronization signal to DSP (PCMSClk), a codec transmit data line (PCMTX) and a codec receive data line (PCMRX). The COBBA-GJ generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA-GJ also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing the RFIClk 13 MHz by 13. The COBBA-GJ further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.



Alert Signal Generation

A buzzer is used for giving alerting tones and/or melodies as a signal of an incoming call. Also keypress and user function response beeps are generated with the buzzer. The buzzer is controlled with a BuzzerPWM output signal from the MAD. A dynamic type of buzzer must be used since the supply voltage available can not produce the required sound pressure for a piezo type buzzer. The low impedance buzzer is connected to an output transistor that gets drive current from the PWM output. The alert volume can be adjusted either by changing the pulse width causing the level to change or by changing the frequency to utilize the resonance frequency range of the buzzer.

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is controlled with a VibraPWM output signal from the MAD2. The vibra alert can be adjusted either by changing the pulse width or by changing the pulse frequency. The vibra device is not inside the phone, but in a special vibra battery.

Digital Control

The baseband functions are controlled by the MAD asic, which consists of a MCU, a system ASIC and a DSP.

MAD2

MAD2 contains following building blocks:

- ARM RISC processor with both 16-bit instruction set (THUMB mode) and 32-bit instruction set (ARM mode)
- TI Lead DSP core with peripherals:
 - API (Arm Port Interface memory) for MCU–DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting
 - Serial port (connection to PCM)
 - Timer
 - DSP memory
- BUSC (BusController for controlling accesses from ARM to API, System Logic and MCU external memories, both 8- and 16-bit memories)
- System Logic
 - CTSI (Clock, Timing, Sleep and Interrupt control)
 - MCUIF (Interface to ARM via BusC). Contains MCU BootROM
 - DSPIF (Interface to DSP)
 - MFI (Interface to COBBA AD/DA Converters)

- CODER (Block encoding/decoding and A51&A52 ciphering)
- AcclF(Accessory Interface)
- SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
- UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
- SIMI (SimCard interface with enhanced features)
- PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)

The MAD2 operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD2 supplies a 6,5MHz or a 13MHz internal clock for the MCU and system logic blocks and a 13MHz clock for the DSP, where it is multiplied to 52 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
1	MCUGenOut5	O	Audio	2	0		MCU General purpose output port
2	MCUGenOut4	O	N101	2	0		MCU General purpose output port
3	<i>LEADGND</i>						Lead Ground
4	MCUGenOut3	O		2	0		MCU General purpose output port
5	VCC					IO VCC in 3325c10	Power
6	MCUGenOut2	O		2	0		MCU General purpose output port
7	MCUGenOut1	O	MCU memory	2	0		MCU General purpose output port
8	MCUGenOut0	O		2	1	LoByteSelX in 16-bit mode	MCU General purpose output port
9	Col4	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 4

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
10	Col3	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 3
11	GND						Ground
12	Col2	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 2
13	Col1	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 1
14	Col0	I/O	UIF	2	Input	programmable pullup PR0201	I/O line for keyboard column 0
15	LCDCSX	I/O	UIF	2	Input	external pullup/down	serial LCD driver chip select, parallel LCD driver enable
16	<i>LEADVCC</i>						Lead Power
17	Row5LCDCD	I/O	UIF	2	Input, pullup	pullup PR0201	Keyboard row5 data I/O , serial LCD driver command/data indicator, parallel LCD driver read/write select
18	VCC					Core VCC in 3325c10	Power
19	Row4	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for keyboard row 4, parallel LCD driver register selection control
20	Row3	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for keyboard row 3, parallel LCD driver data
21	Row2	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for keyboard row 2, parallel LCD driver data
22	Row1	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for keyboard row 1, parallel LCD driver data
23	Row0	I/O	UIF	2	Input, pullup	pullup PR0201	I/O line for keyboard row 0, parallel LCD driver data

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
24	JTDO	O		2	Tri-state		JTAG data out
25	GND						Ground
26	JTRst	I			Input, pull-down	pulldown PD0201	JTAG reset
27	JTCIk	I			Input	pulldown PD0201	JTAG Clock
28	JTDI	I			Input, pullup	pullup PR0201	JTAG data in
29	JTMS	I			Input, pullup	pullup PR0201	JTAG mode select
30	VCC					IO VCC in 3325c10	Power
31	CoEmu0	I/O		2	Input, pullup	pullup PR0201	DSP/MCU emulation port 0
32	CoEmu1	I/O		2	Input, pullup	pullup PR0201	DSP/MCU emulation port 1
33	MCUGenIO7	I/O		2	Input, pull-down	pulldown PD1001	General purpose I/O port
34	MCUGenIO6	I/O	UI	2	Input, pull-down	pulldown PD1001	Lights
35	<i>LEADGND</i>						Lead Ground
36	MCUGenIO5	I/O	UI	2	Input, pull-down	pulldown PD1001	LCD reset
37	<i>ARMGND</i>						ARM Ground
38	MCUAd0	O	MCU MEMORY	2	0		MCU address bus
39	<i>ARMVCC</i>						ARM Power
40	MCUAd1	O	MCU MEMORY	2	0		MCU address bus
41	MCUAd2	O	MCU MEMORY	2	0		MCU address bus
42	GND						Ground
43	MCUAd3	O	MCU MEMORY	2	0		MCU address bus
44	MCUAd4	O	MCU MEMORY	2	0		MCU address bus
45	MCUAd5	O	MCU MEMORY	2	0		MCU address bus

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
46	MCUAd6	O	MCU MEMORY	2	0		MCU address bus
47	VCC					IO VCC in 3325c10	Power
48	MCUAd7	O	MCU MEMORY	2	0		MCU address bus
49	MCUAd8	O	MCU MEMORY	2	0		MCU address bus
50	MCUAd9	O	MCU MEMORY	2	0		MCU address bus
51	MCUAd10	O	MCU MEMORY	2	0		MCU address bus
52	GND						Ground
53	MCUAd11	O	MCU MEMORY	2	0		MCU address bus
54	MCUAd12	O	MCU MEMORY	2	0		MCU address bus
55	MCUAd13	O	MCU MEMORY	2	0		MCU address bus
56	MCUAd14	O	MCU MEMORY	2	0		MCU address bus
57	MCUAd15	O	MCU MEMORY	2	0		MCU address bus
58	MCUAd16	O	MCU MEMORY	2	0		MCU address bus
59	VCC					Core VCC in 3325c10	Power
60	MCUAd17	O	MCU MEMORY	2	0		MCU address bus
61	MCUAd18	O	MCU MEMORY	2	0		MCU address bus
62	MCUAd19	O	MCU MEMORY	2	0		MCU address bus
63	MCUAd20	O	MCU MEMORY	2	0		MCU address bus
64	MCUAd21	O	MCU MEMORY	2	0		MCU address bus
65	ExtMCUDa0	I/O	MCU MEMORY	2	Input		MCU data bus
66	GND						Ground
67	ExtMCUDa1	I/O	MCU MEMORY	2	Output		MCU data bus
68	ExtMCUDa2	I/O	MCU MEMORY	2	Output		MCU data bus

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
69	ExtMCUDa3	I/O	MCU MEMORY	2	Output		MCU data bus
70	ExtMCUDa4	I/O	MCU MEMORY	2	Output		MCU data bus
71	ExtMCUDa5	I/O	MCU MEMORY	2	Output		MCU data bus
72	ExtMCUDa6	I/O	MCU MEMORY	2	Output		MCU data bus
73	VCC					IO VCC in 3325c10	Power
74	ExtMCUDa7	I/O	MCU MEMORY	2	Output		MCU data bus
75	MCUGenIO8	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
76	MCUGenIO9	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
77	MCUGenIO10	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
78	MCUGenIO11	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
79	GND						Ground
80	MCUGenIO12	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
81	MCUGenIO13	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
82	MCUGenIO14	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
83	MCUGenIO15	I/O		2	Input	MCU Data in 16-bit mode	General purpose I/O port
84	MCURdX	O	MCU MEMORY	2	1		MCU Read strobe
85	VCC					Core VCC in 3325c10	Power
86	MCUWrX	O	MCU MEMORY	2	1		MCU write strobe
87	ROM1SelX	O	MCU ROM	2	1		ROM chip select
88	RAMSelX	O	MCU RAM	2	1		RAM chip select
89	ROM2SelX	O	MCU ROM2	2	1		Extra chip select, can be used as MCU general output
90	MCUGenIO1	I/O		2	Input, pullup	pullup PR0201	General purpose I/O port
91	DSPXF	O		2	1		External flag

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
92	SCVCC						Special cell Power
93	RFCIk	I	VCXO		Input		System clock from VCTCXO
94	RFCIkGnd				Input		System clock reference ground input
95	SIMCardDetX	I			Input		SIM card detection
96	SCGND						Special cell Ground
97	BuzzPWM	O	BUZZER	2	0		Buzzer PWM control
98	LEADVCC						LEAD Power
99	VibraPWM	O	VIBRA	2	0		Vibra PWM control
100	GND						Ground
101	MCUGenIO3	I/O	EEPROM	2	Input, pullup	pullup PR1001	General purpose I/O port
102	MCUGenIO2	I/O	EEPROM	2	Input, pullup	pullup PR1001	WP SCL
103	EEPROMSelX	O	MCU EEPROM	2	1		EEPROM chip select, can be used as MCU general output
104	AccTxData	I/O		4	Tri-State	external pullup	Accessory TX data, Flash_TX
105	VCC					IO VCC in 3325c10	Power
106	GenDet	I			Input		General purpose interrupt
107	HookDet	I			Input		Non-MBUS accessory connection detector
108	HeadDet	I			Input		Headset detection interrupt
109	AccRxData	I			Input		Accessory RX data, Flash_RX
110	GND						Ground
111	MCUGenIO4	I/O		2	Input, pull-down	pulldown PD1001	General purpose I/O port

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
112	MBUS	I/O		2	Input, external pullup	external pullup	MBUS, Flash clock
113	VCXOPwr	O	CCONT	2	1		VCXO regulator control
114	SynthPwr	O	CCONT	2	0		Synthesizer regulator control
115	VCC					Core VCC in 3325c10	Power
116	GenCCONTCSX	O	CCONT	2	1		Chip select to CCONT
117	<i>LEADGND</i>						LEAD Ground
118	GenSDIO	I/O	CCONT, UIF	2	Input, external pullup/down	external pullup/down depending on how to boot	Serial data in/out
119	GenSClk	O	CCONT, UIF	2	0		Serial clock
120	SIMCardData	I/O	CCONT	2	0		SIM data
121	GND						Ground
122	PURX	I	CCONT		Input		Power Up Reset
123	CCONTInt	I	CCONT		Input		CCONT interrupt
124	Clk32k	I	CCONT		Input		Sleep clock oscillator input
125	VCC					IO VCC in 3325c10	Power
126	SIMCardClk	O	CCONT	2	0		SIM clock
127	SIMCardRstX	O	CCONT	2	0		SIM reset
128	SIMCardIOC	O	CCONT	2	0		SIM data in/out control
129	SIMCardPwr	O	CCONT	2	0		SIM power control
130	<i>LEADVCC</i>						LEAD Power
131	RxPwr	O	CCONT	2	0		RX regulator control
132	TxPwr	O	CCONT	2	0		TX regulator control
133	TestMode	I			Input, pull-down	pulldown PD0201	Test mode select
134	ExtSysResetX	O		2	0		System Reset

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
135	PCMTxDa	O	COBBA	2	0		Transmit data, DX
136	VCC					IO VCC in 3325c10	Power
137	PCMRxDa	I	COBBA		Input		Receive data, RX
138	PCMDClk	I	COBBA		Input		Transmit clock, CLKX
139	PCMSClk	I	COBBA		Input		Transmitframe sync, FSX
140	COBBADAX	I	COBBA		Input		Data available acknowledge
141	GND						Ground
142	COBBAWrX	O	COBBA	2	1		COBBA write strobe
143	COBBARdX	O	COBBA	2	1		COBBA read strobe
144	COBBAClk	O	COBBA	4	1		COBBA clock, 13 MHz
145	COBBAAa3	O	COBBA	2	0		COBBA address bit
146	COBBAAa2	O	COBBA	2	0		COBBA address bit
147	COBBAAa1	O	COBBA	2	0		COBBA address bit
148	COBBAAa0	O	COBBA	2	0		COBBA address bit
149	COBBADa11	I/O	COBBA	2	0		COBBA data bit
150	VCC					Core VCC in 3325c10	Power
151	COBBADa10	I/O	COBBA	2	0		COBBA data bit
152	COBBADa9	I/O	COBBA	2	0		COBBA data bit
153	COBBADa8	I/O	COBBA	2	0		COBBA data bit
154	COBBADa7	I/O	COBBA	2	0		COBBA data bit
155	COBBADa6	I/O	COBBA	2	0		COBBA data bit
156	GND						Ground
157	COBBADa5	I/O	COBBA	2	0		COBBA data bit
158	COBBADa4	I/O	COBBA	2	0		COBBA data bit
159	COBBADa3	I/O	COBBA	2	0		COBBA data bit
160	COBBADa2	I/O	COBBA	2	0		COBBA data bit
161	COBBADa1	I/O	COBBA	2	0		COBBA data bit

Pin N:o	Pin Name	Pin Type	Connected to/from	Drive req. mA	Reset State	Note	Explanation
162	COBBADa0	I/O	COBBA	2	0		COBBA data bit
163	DSPGenOut5	O	RF	2	0		DSP general purpose output, COBBA reset
164	VCC					IO VCC in 3325c10	Power
165	DSPGenOut4	O		2	0		DSP general purpose output
166	DSPGenOut3	O	IR	2	0		IR ON
167	DSPGenOut2	O		2	0		DSP general purpose output
168	DSPGenOut1	O		2	0		DSP general purpose output
169	DSPGenOut0	O		2	0		DSP general purpose output
170	MCUGenIO0	I/O	EEPROM	2	Input, pullup	pullup PR0201	SDA
171	FrACtrl	O	RF	2	0		SDATX0
172	GND						Ground
173	SynthEna	O	PLUSA	2	0		Synthesizer data enable
174	SynthClk	O	PLUSA	2	0		Synthesizer clock
175	SynthData	O	PLUSA	2	0		Synthesizer data
176	TxPA	O	PLUSA, power amplifier	2	0		Power amplifier control

Memories

The MCU program code resides in an external flash program memory, which size is 8 Mbits (512kx16bit). The MCU work (data) memory size is 512kbits (64kx8bit). A serial EEPROM is used for storing the system and tuning parameters, user settings and selections, a scratch pad and a short code memory. The EEPROM size is 64kbits (8kx8bit).

The BusController (BUSC) section in the MAD decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programmable number of wait states for each memory range.

Program Memory

The MCU program code resides in the program memory. The program memory size is 8 Mbits (512kx16bit).

The flash memory has a power down pin that should be kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

SRAM Memory

The work memory is a static ram of size 512k (64kx8) in a shrink TSOP32 package. The work memory is supplied from the common baseband VBB voltage and the memory contents are lost when the baseband voltage is switched off. All retainable data should be stored into the EEPROM (or flash) when the phone is powered down.

EEPROM Memory

An EEPROM is used for a nonvolatile data memory to store the tuning parameters and phone setup information. The short code memory for storing user defined information is also implemented in the EEPROM. The EEPROM size is 8kbytes. The memory is accessed through a serial bus and the default package is SO8.

MCU Memory Map

MAD2 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 16-bit databus. The BUSC bus controller supports 8- and 16-bit access for byte, double byte, word and double word data. Access wait state 2 and used databus width can be selected separately for each memory block.

Flash Programming

The phone have to be connected to the flash loading adapter FLA-5 so that supply voltage for the phone and data transmission lines can be supplied from/to FLA-5. When FLA-5 switches supply voltage to the phone, the program execution starts from the BOOT ROM and the MCU investigates in the early start-up sequence if the flash prommer is connected. This is done by checking the status of the MBUS-line. Normally this line is high but when the flash prommer is connected the line is forced low by the prommer.

The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX-line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 gets initialized. This must be happened within 15 ms after TX line is pulled low. After that the data transfer of the first two bytes from the flash prommer to the baseband on the RX-line must be done within 1 ms.

When MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word. If these timeout values are exceeded, the MCU (MAD2) starts normal code execution from flash. After this, the timing between the phone and the flash prommer is handled with dummy bites.

A 5V programming voltage is supplied inside the transceiver from the battery voltage with a switch mode regulator (5V/30mA) of the CCONT. The 5V is connected to VPP pin of the flash through the UI board.

COBBA-GJ

The COBBA-GJ provides an interface between the baseband and the RF-circuitry. COBBA-GJ performs analogue to digital conversion of the receive signal. For transmit path COBBA_GJ performs digital to analogue conversion of the transmit amplifier power control ramp and the in-phase and quadrature signals. A slow speed digital to analogue converter will provide automatic frequency control (AFC).

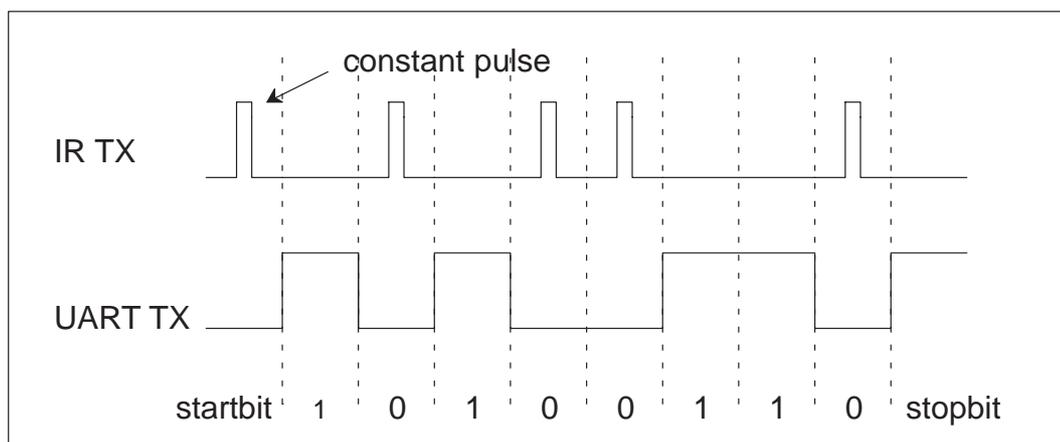
The COBBA asic is at any time connected to MAD asic with two interfaces, one for transferring tx and rx data between MAD and COBBA and one for transferring codec rx/tx samples.

Infrared Transceiver Module

The module is activated with an IRON signal by the MAD, which supplies power to the module. The IR datalines are connected to the MAD accessory interface Acclf via FBUS. The RX and TX lines are separated from FBUS by three-state buffers, when the IR-module is switched off. The Acclf in MAD performs pulse encoding and shaping for transmitted data and detection and decoding for received data pulses.

The data is transferred over the IR link using serial data at speeds 9.6, 19.2, 38.4, 57.6 or 115.2 kbits/s, which leads to maximum throughput of 92.160 kbits/s. The used IR module complies with the IrDA 1.0 specification (Infra Red Data Association), which is based on the HP SIR (Hewlett-Packard's Serial Infra Red) concept.

Following figure gives an example of IR transmission pulses. In IR transmission a light pulse corresponds to 0-bit and a "dark pulse" corresponds to 1-bit.



The FBUS cannot be used for external accessory communication when the infrared mode is selected, as IR communication reserves the FBUS completely.

Real Time Clock

Requirements for a real time clock implementation are a basic clock (hours and minutes), a calendar and a timer with alarm and power on/off-function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) will be implemented with the MCU software. The RTC needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargeable polyacene battery that can keep the clock running some ten minutes. If the backup has expired, the RTC clock restarts after the main battery is connected. The CCONT keeps MCU in reset until the 32kHz source is settled (1s max).

The CCONT is an ideal place for an integrated real time clock as the asic already contains the power up/down functions and a sleep control with the 32kHz sleep clock, which is running always when the phone battery is connected. This sleep clock is used for a time source to a RTC block.

RTC backup battery charging

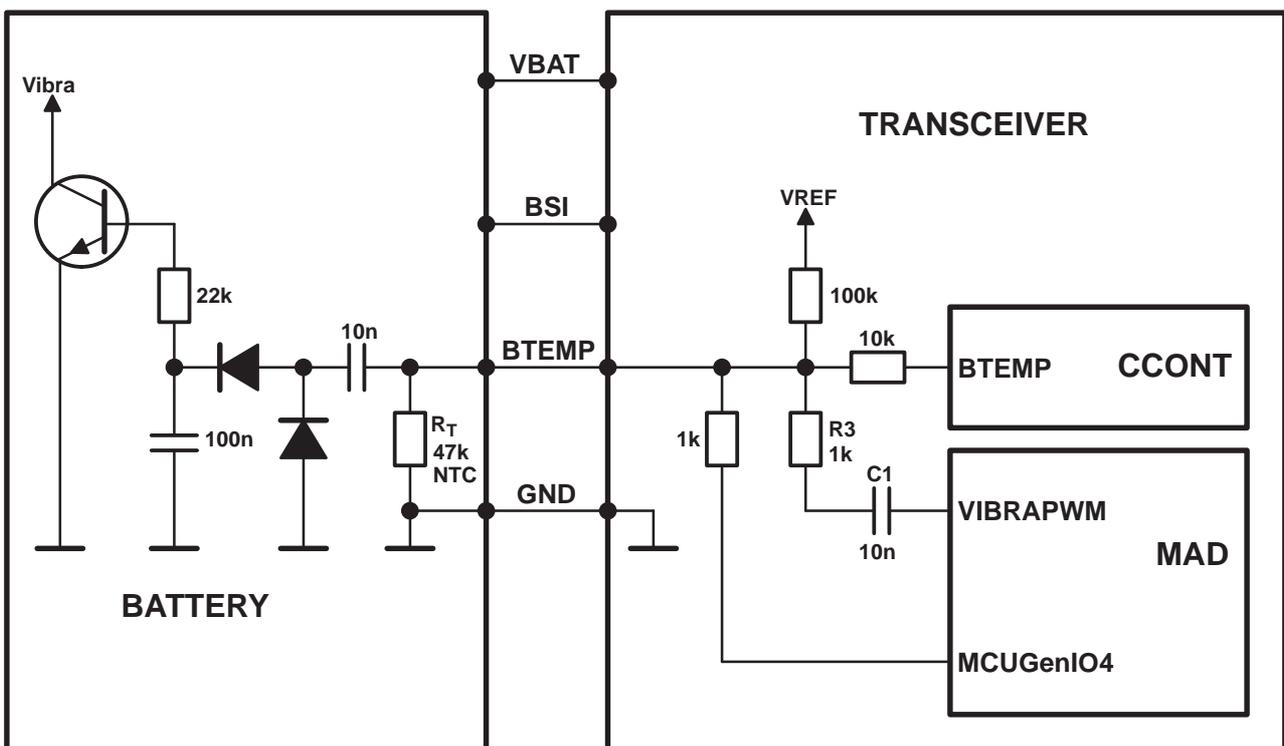
CHAPS has a current limited voltage regulator for charging a backup battery. The regulator derives its power from VOUT so that charging can take place without the need to connect a charger. The backup battery is only used to provide power to a real time clock when VOUT is not present so it is important that power to the charging circuitry is derived from VOUT and that the charging circuitry does not present a load to the backup battery when VOUT is not present.

It should not be possible for charging current to flow from the backup battery into VOUT if VOUT happens to be lower than VBACK. Charging current will gradually diminish as the backup battery voltage reaches that of the regulation voltage.

Vibra Alerting Device

A vibra alerting device is used for giving silent signal to the user of an incoming call. The device is not placed in the phone but it will be added to a special battery pack. The vibra is controlled with a PWM signal by the MAD via the BTEMP battery terminal.

A 15kohm BSI resistor is needed to detect the vibra battery. It is only used to enable vibra selection in user menu. When alerting, VibraPWM signal is delivered to battery.



IBI Accessories

All accessories which can be connected between the transceiver and the battery or which itself contain the battery, are called IBI accessories.

Either the phone or the IBI accessory can turn the other on, but both possibilities are not allowed in the same accessory.

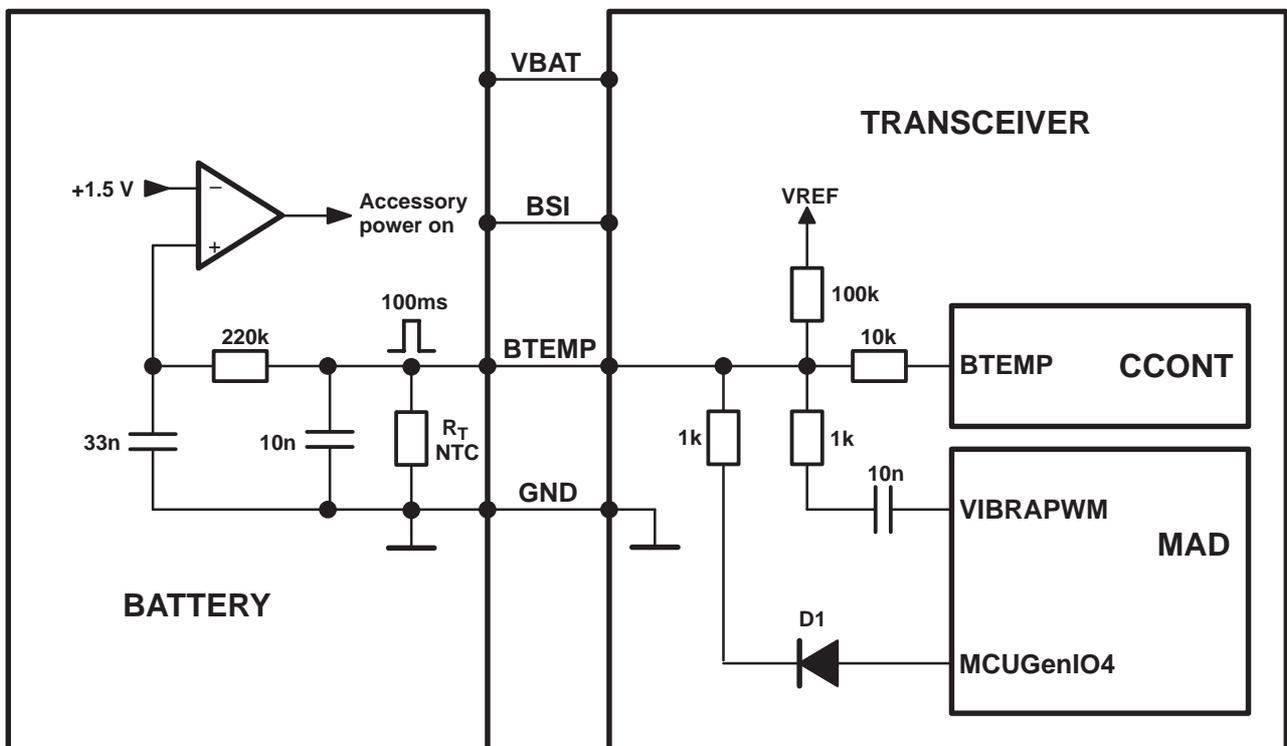
Phone Power-on by IBI

IBI accessory can power the phone on by pulling the BTEMP line up to 3 V.

IBI power-on by phone

Phone can power the IBI accessory on by pulling the BTEMP line up by MCUGenIO4 of MAD2. BTEMP measurement is not possible during this time.

The accessory is commanded back to power-off by MBUS message.

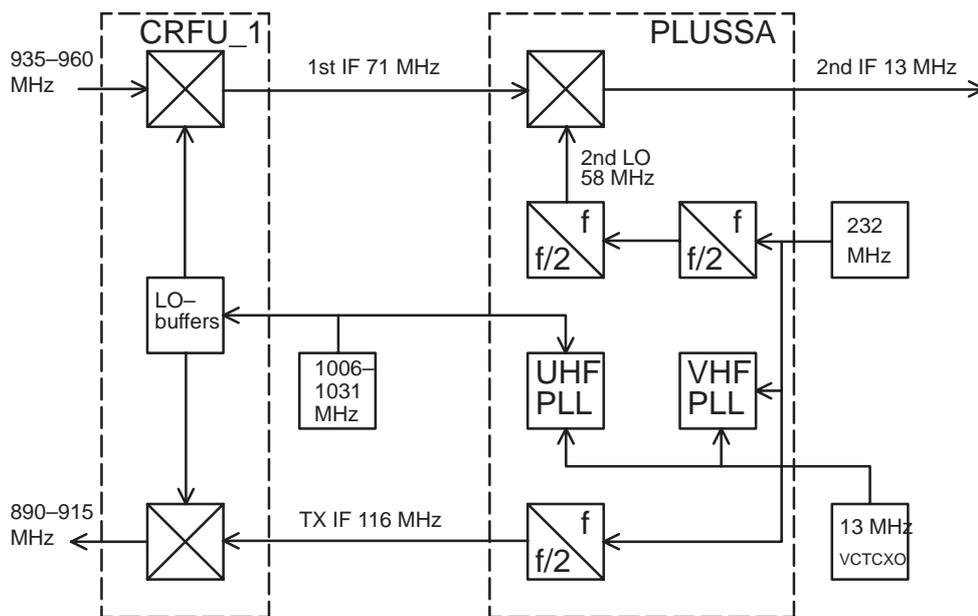


RF Module

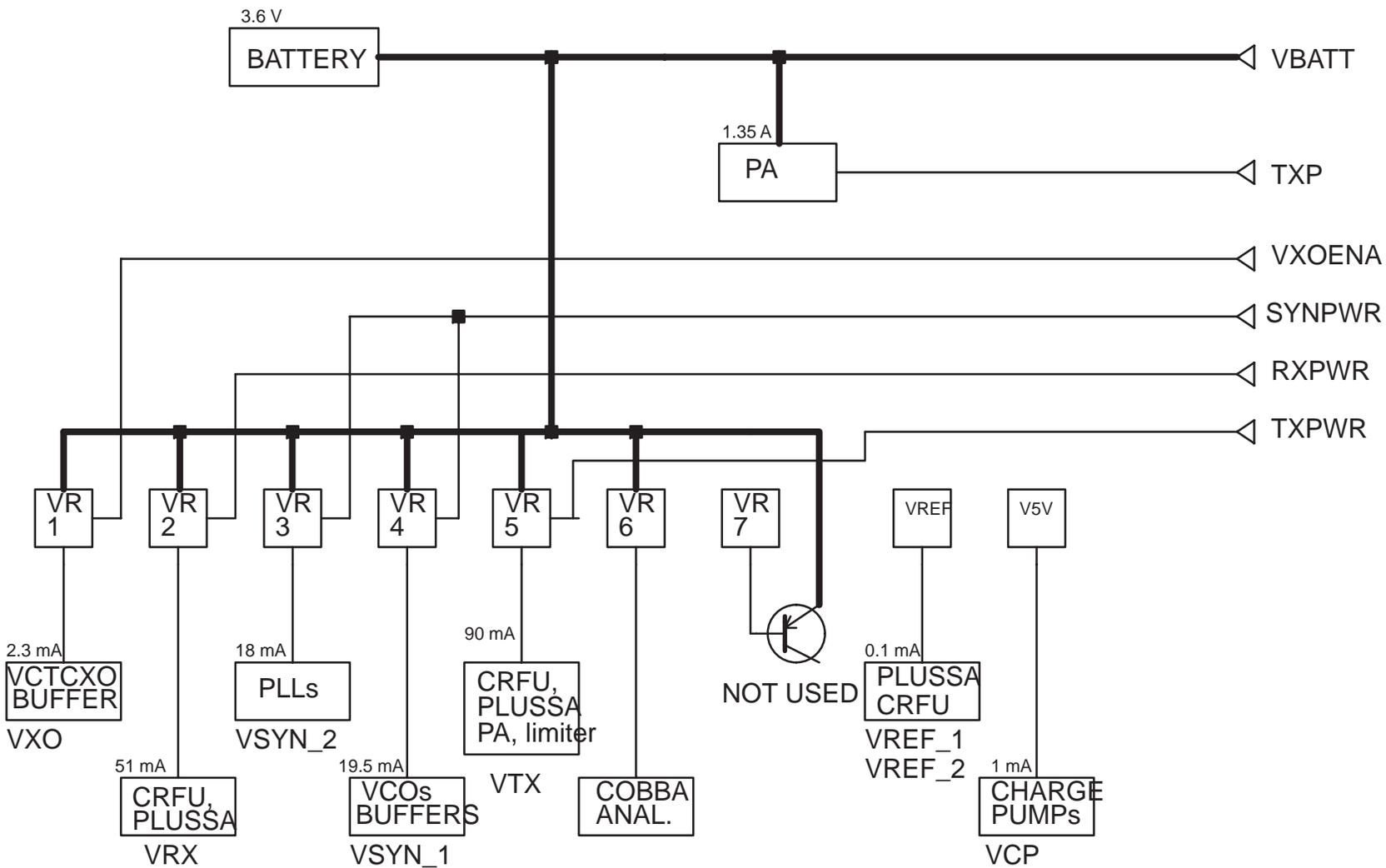
Maximum Ratings

Parameter	Rating
Battery voltage, idle mode	6.0 V
Battery voltage during call, highest power level	5.0 V
Regulated supply voltage	2.8 +/- 3% V
Voltage reference	1.5 +/- 1.5% V
Operating temperature range	-10...+55 deg. C

RF Frequency Plan



Power Distribution Diagram



DC Characteristics

Regulators

Transceiver has got a multi function power management IC, which contains among other functions, also 7 pcs of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register. In GSM direct controls are used to get fast switching, because regulators are used to enable RF-functions.

Use of the regulators can be seen in the power distribution diagram.

CCONT also provides 1.5 V reference voltage for PLUSSA and CRFU1a (and for DACs and ADCs in COBBA too).

Control Signals

All control signals are coming from MAD and they are 2.8 V logic signals.

Functional Description

RF block diagram has conventional dual conversion receiver and in transmitter there is a upconversion mixer for the final TX-frequency.

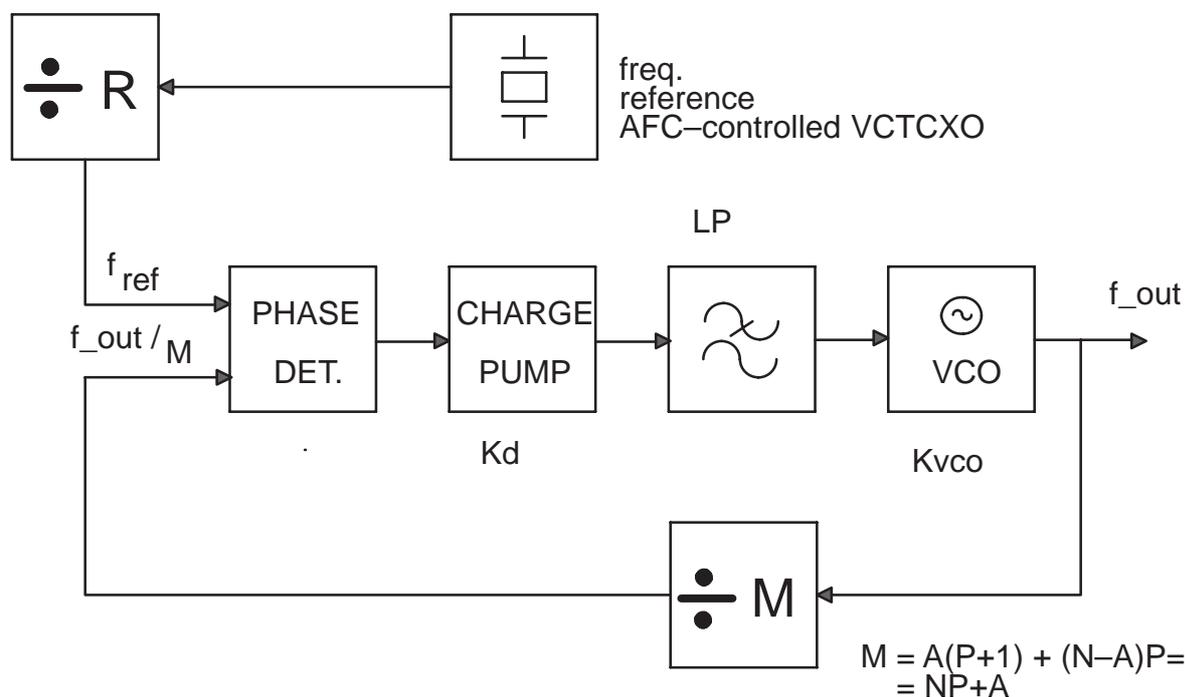
Architecture contains three ICs. Most of the functions are horizontally and vertically integrated. UHF functions except power amplifier and VCO are integrated into CRFU_1a, which is a BiCMOS-circuit suitable for LNA- and mixer-function. Most of the functions are in PLUSSA, which also is a BiCMOS-circuit. PLUSSA is a IF-circuit including IQ-modulator and PLLs for VHF- and UHF-synthesizers.

Power amplifier is also an ASIC, it is a so called MMIC (monolithic microwave integrated circuit). It has three amplifier stages including input and interstage matchings. Output matching network is external. Also TX gain control is integrated into this chip.

Frequency synthesizers

Both VCOs are locked with PLLs into stable frequency source (see figure 3), which is a VCTCXO-module (voltage controlled temperature compensated crystal oscillator). VCTCXO is running at 13 MHz. Temperature effect is controlled with AFC (automatic frequency control) voltage, VCTCXO is locked into frequency of the base station. AFC is generated by baseband with a 11 bit conventional DAC in COBBA.

UHF PLL is located into PLUSSA. There is 64/65 ($P/P+1$) prescaler, N- and A-divider, reference divider, phase detector and charge pump for the external loop filter. UHF local signal is generated by a VCO-module (VCO = voltage controlled oscillator) and sample of frequency of VCO is fed to prescaler. Prescaler is a dual modulus divider. Output of the prescaler is fed to N- and A-divider, which produce the input to phase detector. Phase detector compares this signal to reference signal, which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency. Loop filter filters out the pulses and generates DC to control the frequency of UHF-VCO. Loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that's why integrator capacitor has got a resistor for phase compensation. Other filter components are for sideband rejection. Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into dividers. HF-synthesizer is the channel synthesizer, so the channel spacing is 200 kHz. 200 kHz is reference frequency for the phase detector.



VHF PLL is also located into PLUSSA. There is 16/17 ($P/P+1$) dual modulus prescaler, N- and A-dividers, reference divider, phase detector and charge pump for the loop filter. VHF local signal is generated with a discrete VCO-circuit. VHF PLL works in the same way as UHF-PLL. VHF-PLL is locked on fixed frequency, so higher reference frequency is used to decrease phase noise.

Receiver

Receiver is a dual conversion linear receiver.

Received RF-signal from the antenna is fed via the duplex filter to LNA (low noise amplifier) in CRFU_1a. Active parts (RF-transistor and biasing and AGC-step circuitry) are integrated into this chip. Input and output matching networks are external. Gain selection is done with PDATA0 control. Gain step in LNA is activated when RF-level in antenna is about -45 dBm. After the LNA amplified signal (with low noise level) is fed to bandpass filter, which is a SAW-filter (SAW, surface acoustic wave). Duplex filter and RX interstage bandpass filters together define, how good are the blocking characteristics against spurious signals outside receive band and the protection against spurious responses, mainly the image of the first mixer.

This bandpass filtered signal is then mixed down to 71 MHz, which is first intermediate frequency. 1st mixer is located into CRFU_1a ASIC. This integrated mixer is a double balanced Gilbert cell. All active parts and biasing are integrated and matching components are external. Because this is an active mixer it also amplifies IF-frequency. Also local signal buffering is integrated and upper side injection is used. First local signal is generated with UHF-synthesizer.

First IF-signal is then bandpass filtered with a selective SAW-filter. From the mixer output to IF-circuit input signal path is balanced. IF-filter provides selectivity for channels greater than +/-200 kHz. Also it attenuates image frequency of the second mixer and intermodulating signals. Selectivity is required in this place, because of needed linearity and adjacent channel interferers will be on too high signal level for the stages following.

Next stage in the receiver chain is AGC-amplifier. It is integrated into PLUSSA-ASIC. AGC has analog gain control. Control voltage for the AGC is generated with DA-converter in COBBA in baseband. AGC-stage provides accurate gain control range (min. 60 dB) for the receiver. After the AGC there is second mixer, which generates second intermediate frequency, 13 MHz. Local signal is generated in PLUSSA by dividing VHF-synthesizer output (232 MHz) by four, so the 2nd LO-frequency is 58 MHz.

2nd IF-filter is a ceramic bandpass filter at 13 MHz. It attenuates adjacent channels, except for +/- 200 kHz there is not much attenuation. Those +/- 200 kHz interferers are filtered digitally by the baseband. So RX DACs are so good, that there is enough dynamic range for the faded 200 kHz interferer. Also the whole RX has to be able to handle signal levels in a linear way. After the 13 MHz filter there is a buffer for the IF-signal, which also converts and amplifies single ended signal from filter to balanced signal for the buffer and AD-converters in COBBA. Buffer in PLUSSA has got voltage gain of 36 dB and buffer gain setting in COBBA is 0 dB. It is possible to set gainstep (9.5 dB) into COBBA via control bus, if needed.

Transmitter

Transmitter chain consists of IQ-modulator, upconversion mixer, power amplifier and there is a power control loop.

I- and Q-signals are generated by baseband also in COBBA-ASIC. After post filtering (RC-network) they go into IQ-modulator in PLUSA. It generates modulated TX IF-frequency, which is VHF-synthesizer output divided by two, meaning 116 MHz. There is also an AGC-amplifier in PLUSA, but it is not used in GSM. Output is set to maximum with a 5-bit message in control register. AGC-amplifier is used in other digital systems, because PLUSA is a core IC. After PLUSA signal is attenuated and filtered for upconversion into final TX-frequency in CRFU_1a. Upconversion mixer in CRFU_1a is a so called image reject mixer. It is able to attenuate unwanted sideband in the upconverter output. Mixer itself is a double balanced Gilbert cell. Phase shifters required for image rejection are also integrated. Local signal needed in upconversion is generated by the UHF-synthesizer, but buffers for the mixer are integrated into CRFU_1a. Output of the upconverter is buffered and matching network makes a single ended 50 ohm impedance.

Next stage is TX interstage filter, which attenuates unwanted signals from the upconverter, mainly LO-leakage and image frequency from the upconverter. Also it attenuates wideband noise. This bandpass filter is a SAW-filter.

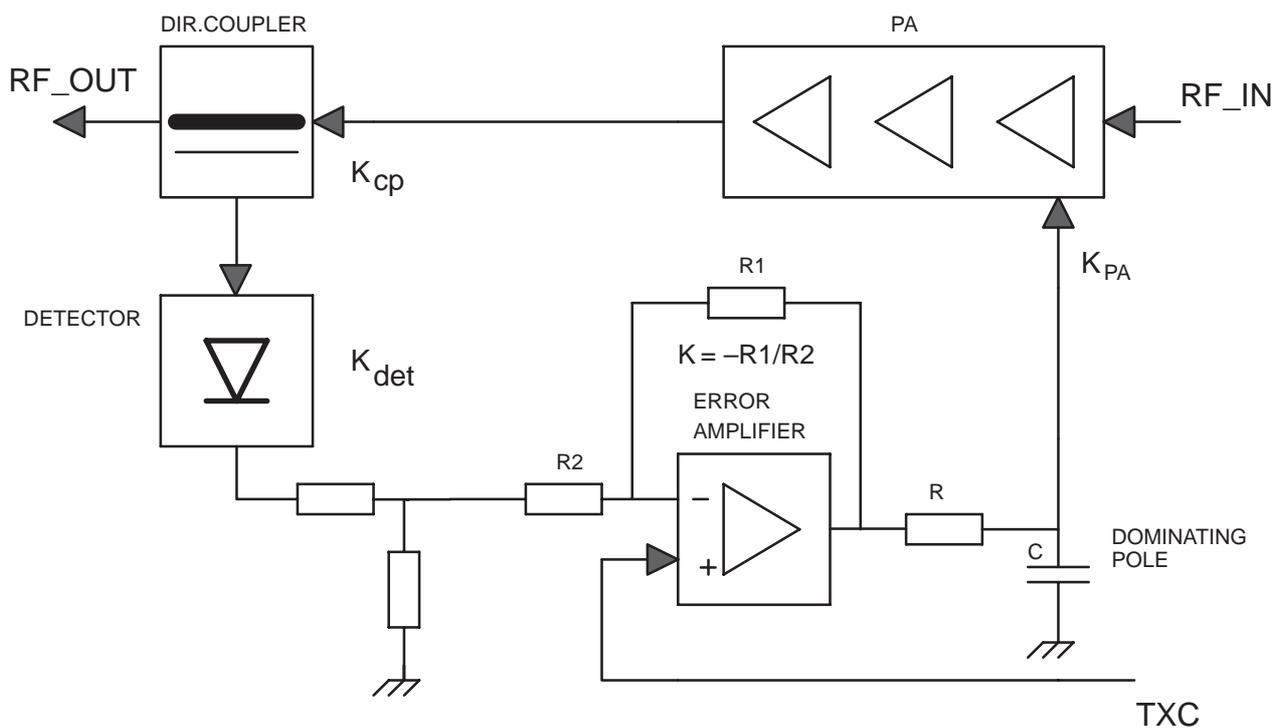
After TX SAW-filter, there is a discrete transistor stage. Function of this block is to reduce the AM-content. This feature is realized with saturated operation of the V640 transistor. Typical input level into this amplifier is higher than output level.

The final amplification is realized with third IC, power amplifier is a MMIC. It has got a 50 ohm input, output requires an external matching network. MMIC contains three amplifier stages and interstage matchings. Also there is a gain control, which is controlled with a power control loop. PA has got over 35 dB power gain and it is able to produce 2.5 W into output with 0 dBm input level. Gain control range is over 35 dB to get desired power levels and power ramping up and down.

Harmonics generated by the nonlinear PA (class AB) are filtered out with the matching network and lowpass/bandstop filtering in the duplexer. Bandstop is required because of wideband noise located on RX-band.

Power control circuitry consists of power detector in the PA output and error amplifier in PLUSA. There is a directional coupler connected between PA output and duplex filter. It takes a sample from the forward going power with certain ratio. This signal is rectified in a schottky-diode and it produces a DC-signal signal after filtering. This peak-detector is linear on absolute scale, except it saturates on very low and high power levels – it produces a S-shape curve.

This detected voltage is compared in the error-amplifier in PLUSSA to TXC-voltage, which is generated by DA-converter in COBBA. Because also gain control characteristics in PA are linear in absolute scale, control loop defines a voltage loop, when closed. Closed loop tracks the TXC-voltage quite linearly. TXC has got a raised cosine form (\cos^4 - function), which reduces switching transients, when pulsing power up and down. Because dynamic range of the detector is not wide enough to control the power (actually RF output voltage) over the whole range, there is a control named TXP to work under detected levels. Burst is enabled and set to rise with TXP until the output level is high enough, that feedback loop works. Loop controls the output via the control pin in PA MMIC to the desired output level and burst has got the waveform of TXC-ramps. Because feedback loops could be unstable, this loop is compensated with a dominating pole. This pole decreases gain on higher frequencies to get phase margins high enough.



AGC strategy

AGC–amplifier is used to maintain output level of the receiver almost constant. AGC has to be set before each received burst, this is called pre–monitoring. Receiver is switched on roughly 150 ms before the burst begins, DSP measures received signal level and adjusts RXC, which controls RX AGC–amplifier or it switches off the LNA with PDATA0 control line. This pre–monitoring is done in three phases and this sets the settling times for RX AGC. Pre–monitoring is required because of linear receiver, received signal must be in full swing, no clipping is allowed and because DSP doesn't know, what is the level going to be in next burst.

There is at least 60 dB accurate gain control (continuous, analog) and one digital step in LNA. It is typically about 30...35 dB.

RSSI must be measured on range –48...–110 dBm. After –48 dBm level MS reports to base station the same reading.

Because of RSSI–requirements, gain step in LNA is used roughly on –45 dBm RF–level and up to –10 dBm input RF–level accurate AGC is used to set RX output level. LNA is ON below –45 dBm. from –45 dBm down to –95 dBm this accurate AGC in PLUSSA is used to adjust the gain to desired value. RSSI–function is in DSP, but it works out received signal level by measuring RX IQ–level after all selectivity filtering (meaning IF–filters, $\Sigma\Delta$ –converter and FIR–filter in DSP). So 50 dB accurate AGC dynamic range is required. Remaining 10 dB is for gain variations in RX–chain (for calibration). Below –95 dBm RF–levels, output level of the receiver drops dB by dB. At –95 dBm level output of the receiver gives 50 mVpp differentially. This is the target value for DSP. Below this it drops down to ca. 9 mVpp differentially @ –110 dBm RF–level.

This strategy is chosen because we have to roll off the AGC in PLUSSA early enough, that it won't saturate in selectivity tests. Also we can't start too early, then we will sacrifice the signal to noise ratio and it would require more accurate AGC dynamic range. 50 mVpp target level is set, because RX–DAC will saturate at 1.4 Vpp. This over 28 dB headroom is required to have margin for +/- 200 kHz faded adjacent channel (ca. 19 dB) and extra 9 dB for pre–monitoring.

Production calibration is done with two RF–levels, LNA gain step is not calibrated. Gain changes in the receiver are taken off from the dynamic range of accurate AGC. Variable gain stage in PLUSSA is designed in a way, that it is capable of compensating itself, there is good enough margin in AGC.

AFC function

AFC is used to lock the transceivers clock to frequency of the base station. AFC-voltage is generated in COBBA with 11 bit AD-converter. There is a RC-filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC-network comes from signaling, how often PSW (pure sine wave) slots occur. They are repeated after 10 frames , meaning that there is PSW in every 46 ms. AFC tracks base station frequency continuously, so transceiver has got a stable frequency, because changes in VCTCXO-output don't occur so fast (temperature). Settling time requirement comes also from the start up-time allowed. When transceiver is in sleep mode and "wakes" up to receive mode , there is only about 5 ms for the AFC-voltage to settle. When the first burst comes in system clock has to be settled into +/- 0.1 ppm frequency accuracy. The VCTCXO-module requires also 5 ms to settle into final frequency. Amplitude rises into full swing in 1 ... 2 ms, but frequency settling time is higher so this oscillator must be powered up early enough.

Receiver blocks

RX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	935 – 960			MHz
Insertion loss			3.8	dB
Maximum drive level			+10	dBm

1st mixer in CRFU_1a

Parameter	Min.	Typ./ Nom.	Max.	Unit/Notes
Supply voltage	2.7	2.8	2.85	V
RX frequency range	935		960	MHz
LO frequency range	1006		1031	MHz
IF frequency		71		MHz
Output resistance (balanced)	10 k			ohm

1st IF-filter

Parameter	min.	typ.	max.	unit
Operating temperature range	-20		+75	deg.C
Center frequency , fo		71		MHz
Maximum ins. loss at 1dB BW			11	dB

Transmitter Blocks

TX interstage filter

Parameter	Min.	Typ.	Max.	Unit
Passband	890 – 915			MHz
Insertion loss			3.8	dB

Power amplifier MMIC

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range			880		915	MHz
Supply voltage	Vcc		3.1	3.5	5.0	V
Gain control range (overall dynamic range)		V _{pc} = 0.5 ... 2.2 V	45			dB

Synthesizer blocks

VHF VCO and low pass filter

Parameter	Min.	Typ.	Max.	Unit/Notes
Supply voltage range	2.7	2.8	2.58	V
Current consumption		4	7	mA
Control voltage	0.5		4.0	V
Operation frequency		232		MHz
Output level	-13	-10		dBm (output after the lowpass filter)

UHF PLL

UHF PLL block in PLUSSA

Parameter	Min.	Typ.	Max.	Unit/notes
Input frequency range	650		1300	MHz
Reference input level	100			mVpp
Reference input frequency			30	MHz
Reference input impedance		tbd.		

UHF VCO module

Parameter	Conditions	Rating	Unit/Notes
Supply voltage, V_{cc}		2.8 +/- 0.1	V
Supply current, I_{cc}	$V_{cc} = 2.8$ V, $V_c = 2.25$ V	< 10	mA
Control voltage, V_c	$V_{cc} = 2.8$ V	0.8... 3.7	V
Oscillation frequency	$V_{cc} = 2.8$ V $V_c = 0.8$ V $V_c = 3.7$ V	< 1006 > 1031	MHz MHz
Tuning voltage in center frequency	$f = 1018.5$ MHz	2.25 +/- 0.25	V
Tuning voltage sensitivity in operating frequency range on each spot freq.	$V_{cc} = 2.8$ V $f = 1006...1031$ MHz	14 +/- 2	MHz/V
Output power level	$V_{cc} = 2.7$ V $f = 1006...1031$ MHz	-6.0 min.	dBm

UHF local signal input in CRFU_1a

Parameter	Min.	Typ.	Max.	Unit/Notes
Input frequency range	990		1040	MHz
Input level	200		700	mVpp

Connections**RF connector and antenna switch**

Parameter	Min.	Typ.	Max.	Unit/Notes
Operating frequency range	890		960	MHz
Insertion loss, COM to INT			0.2	dB
Insertion loss, COM to EXT			0.4	dB
Nominal impedance		50		ohm
Return loss			15	

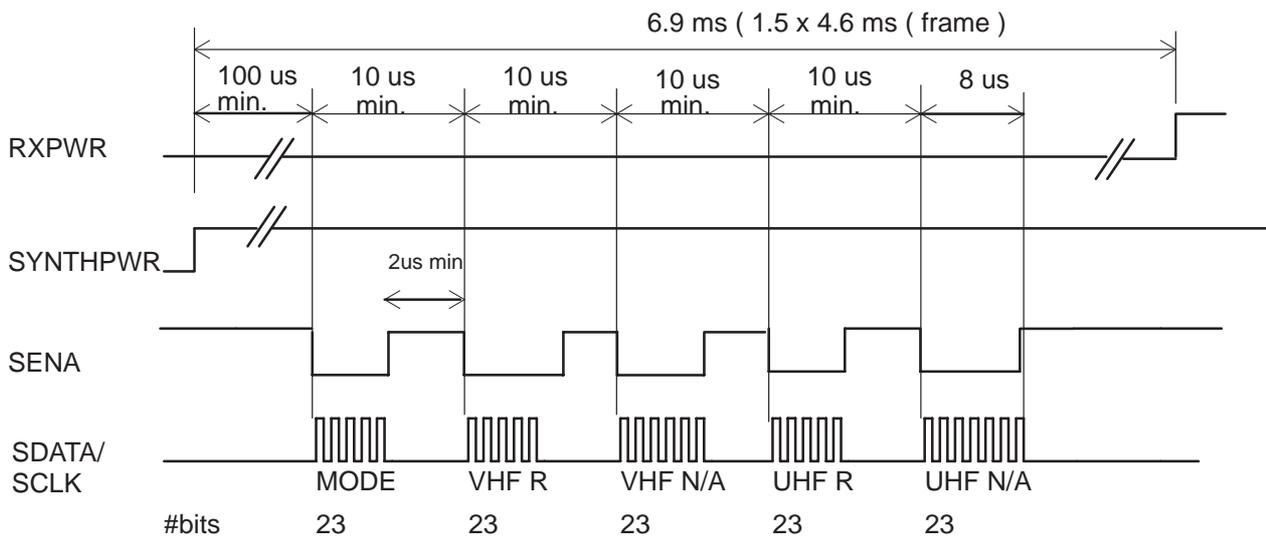
Signal name	From	To	Parameter	Minimum	Typical	Maximum	Unit	Function
VBATT	Battery	RF	Voltage	3.0	3.6	5.0/6.0	V	Supply voltage for RF
VXOE-NA	MAD	CCONT	Logic high "1"	2.0		2.85	V	VR1, VR6 in CCONT ON
			Logic low "0"	0		0.8	V	VR1, VR6 in CCONT OFF

Signal name	From	To	Parameter	Minimum	Typical	Maximum	Unit	Function
SYNPWR	MAD	CCONT	Logic high "1"	2.0		2.85	V	VR3, VR4 in CCONT ON
			Logic low "0"	0		0.8	V	VR3,VR4 in CCONT OFF
RXPWR	MAD	CCONT	Logic high "1"	2.0		2.85	V	VR2, VR5 in CCONT ON
			Logic low "0"	0		0.8	V	VR2, VR5 in CCONT OFF
TXPWR	MAD	CCONT	Logic high "1"	2.0		2.85	V	VR7 in CCONT ON
			Logic low "0"	0		0.8	V	VR7 in CCONT OFF
VREF	CCONT	PLUSSA	Voltage	1.478	1.5	1.523	V	Reference voltage for PLUSSA and CRFU1a
PDATA0	MAD	CRFU_1a	Logic high "1"	2.0		2.85	V	Nominal gain in LNA
			Logic low "0"	0		0.8	V	Reduced gain in LNA
SENA1	MAD	PLUSSA	Logic high "1"	2.0		2.85	V	PLL enable
			Logic low "0"	0		0.8	V	
SDATA	MAD	PLUSSA	Logic high "1"	2.0		2.85	V	Synthesizer data
			Logic low "0"	0		0.8	V	
SCLK	MAD	PLUSSA	Logic high "1"	2.0		2.85	V	Synthesizer clock
			Logic low "0"	0		0.8	V	
AFC	COBBA	VCTCXO	Voltage	0.046		2.254	V	Automatic frequency control signal for VC(TC)XO
RFC	VCTCXO	MAD	Frequency		13		MHz	High stability clock signal for the logic circuits
			Signal amplitude	0.5	1.0	2.0	Vpp	
RXIP/RXIN	PLUSA	COBBA	Output level		50	1344	mVpp	Differential RX 13 MHz signal to baseband
TXIP/TXIN	COBBA	PLUSSA	Differential voltage swing	0.75 x 1.022	0.75 x 1.1	0.75 x 1.18	Vpp	Differential in-phase TX baseband signal for the RF modulator
			DC level	0.784	0.8	0.816	V	
TXQP/TXQN	COBBA	PLUSSA	Differential voltage swing	0.75 x 1.022	0.75 x 1.1	0.75 x 1.18	Vpp	Differential quadrature phase TX baseband signal for the RF modulator
			DC level	0.784	0.8	0.816	V	

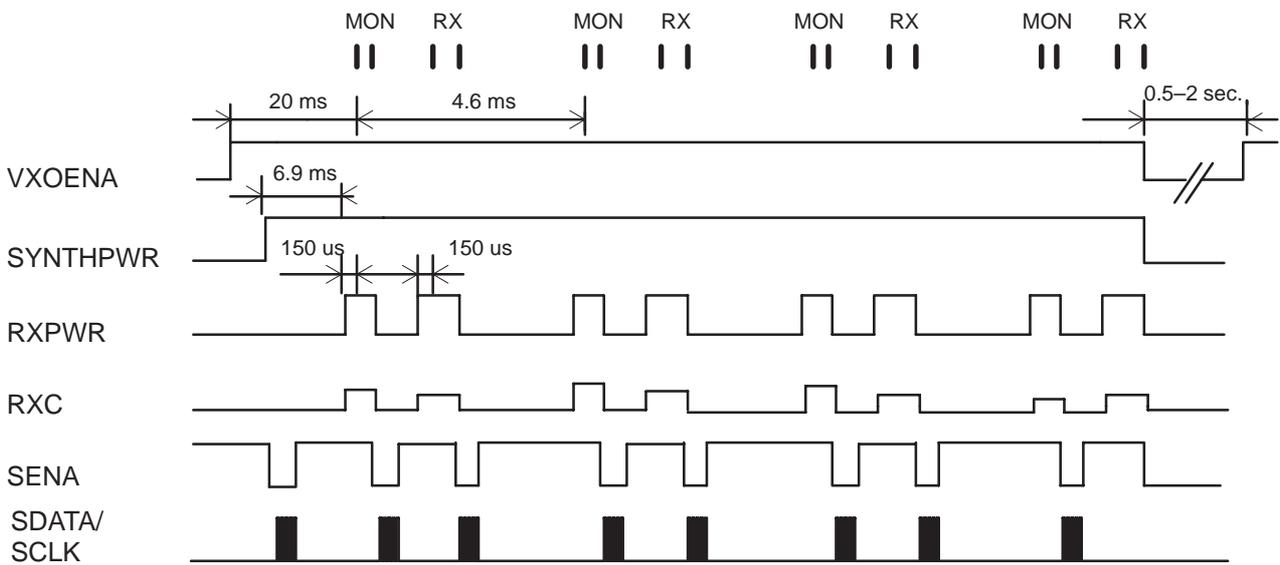
Signal name	From	To	Parameter	Minimum	Typical	Maximum	Unit	Function
TXP	MAD	PLUSA	Logic high "1"	2.0		2.85	V	Transmitter power control enable
			Logic low "0"	0		0.8	V	
TXC	COB-BA	PLUSA	Voltage Min	0.12		0.18	V	Transmitter power control
			Voltage Max	2.27		2.33	V	
RXC	COB-BA	PLUSA	Voltage Min	0.12		0.18	V	Receiver gain control
			Voltage Max	2.27		2.33	V	

Timings

Synthesizer control timing

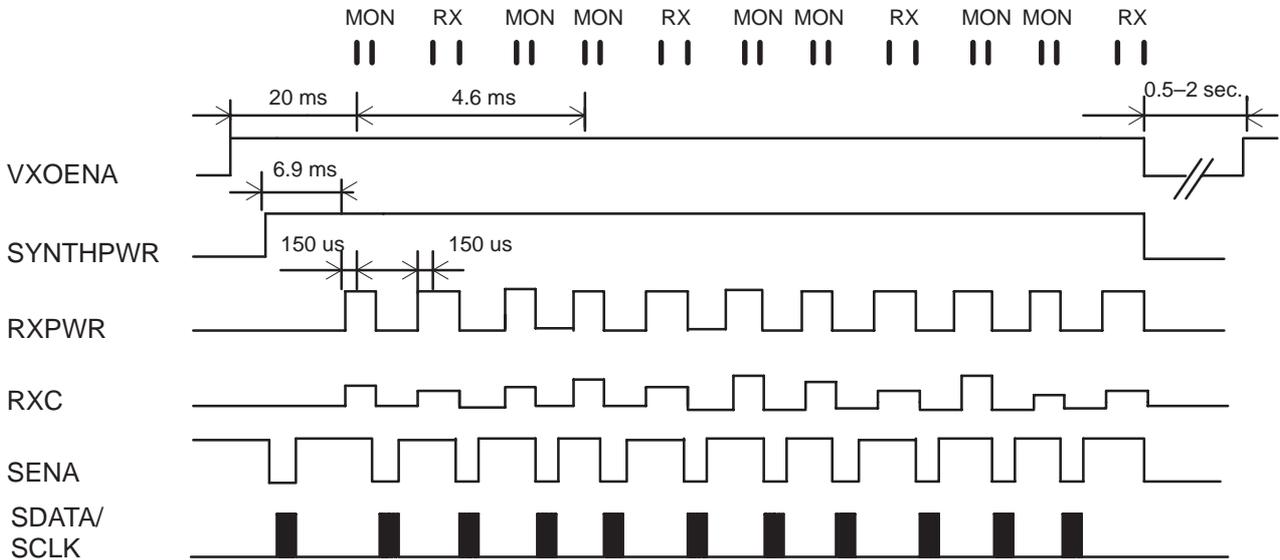


Synthesizer Start-up Timing / clocking

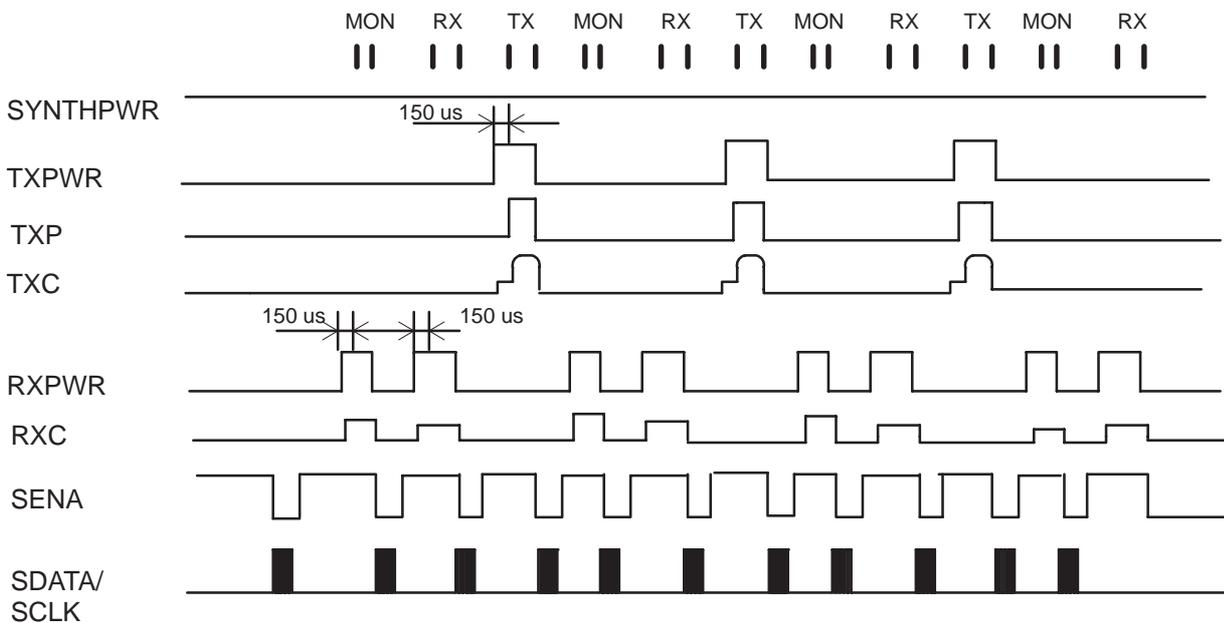


Synthesizer Timing / IDLE,
one monitoring frame,
frame can start also from RX-burst

In case of long list of adjacent channels, there might be two monitoring-bursts/frame. Extra monitoring "replaces" TX-burst.

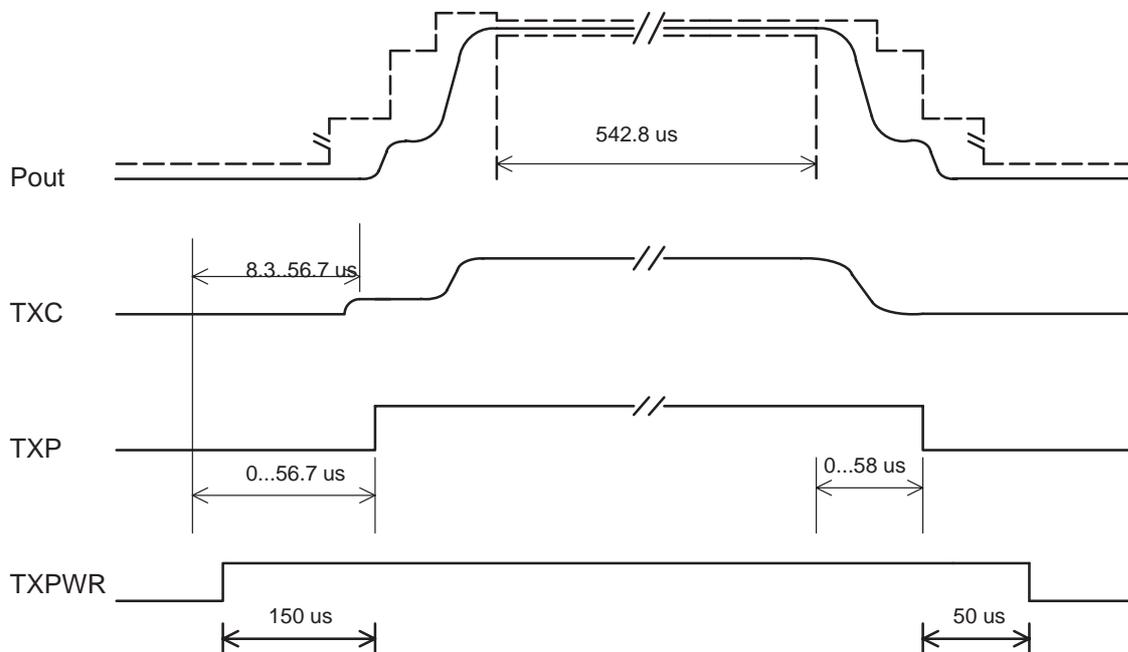


Synthesizer Timing / IDLE 2, frame can start from RX-burst



Synthesizer Timing / traffic channel

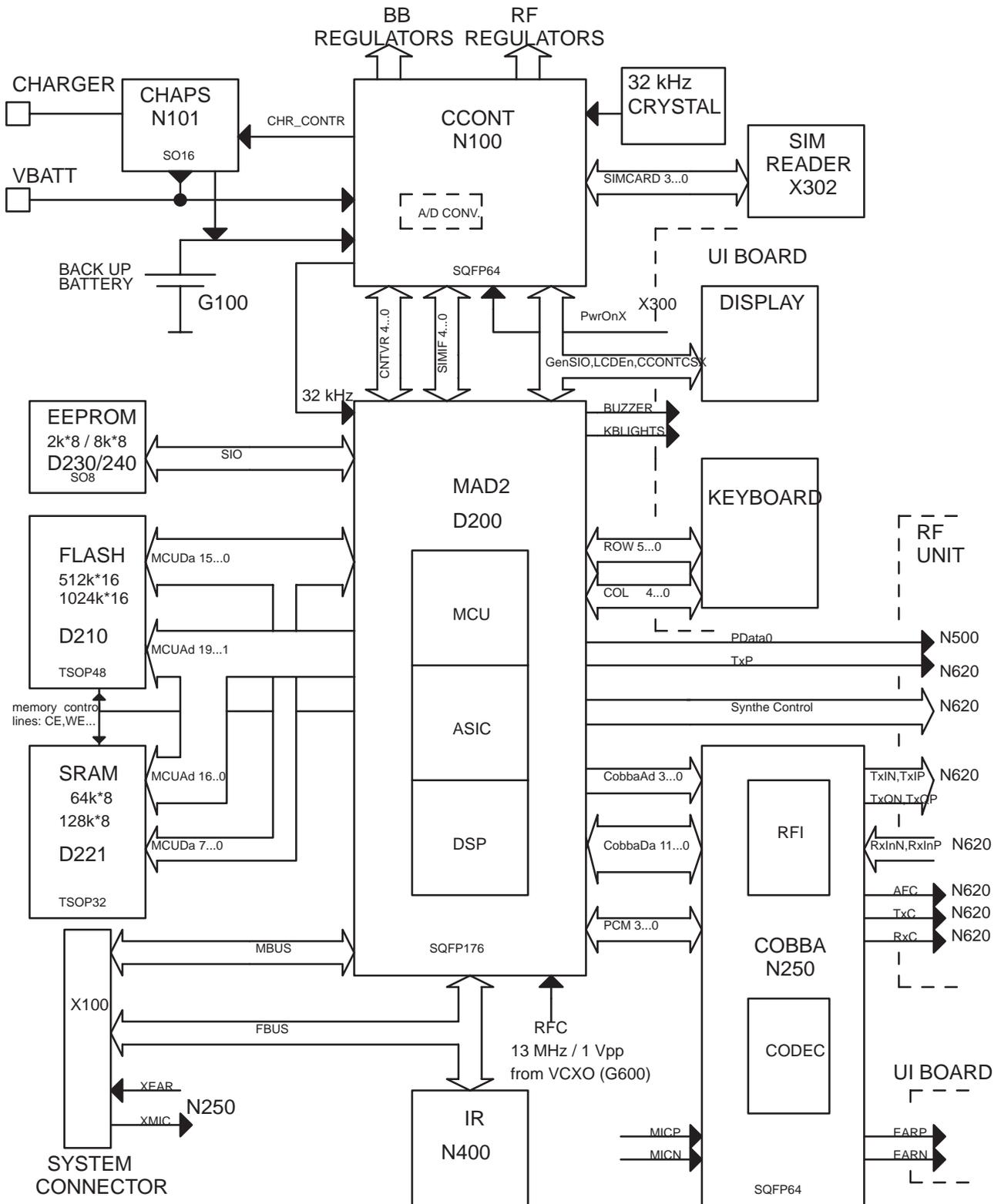
Transmitter power switching timing diagram



Synthesizer clocking

Synthesizers are controlled via serial control bus, which consists of SDA-TA, SCLK and SENA1 signals. These lines form a synchronous data transfer line. SDATA is for the data bits, SCLK is 3.25 MHz clock and SENA1 is latch enable, which stores the data into counters or registers.

Block Diagram of Baseband Blocks



Parts list of UP8T (EDMS Issue 11.11)

Code: 0200951

ITEM	CODE	DESCRIPTION	VALUE	TYPE
R100	1430826	Chip resistor	680 k	5 % 0.063 W 0402
R102	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R103	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R104	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R109	1620017	Res network 0w06 2x100r j	0404	0404
R113	1430726	Chip resistor	100	5 % 0.063 W 0402
R116	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R118	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R120	1620025	Res network 0w06 2x100k j	0404	0404
R122	1620019	Res network 0w06 2x10k j	0404	0404
R124	1620017	Res network 0w06 2x100r j	0404	0404
R127	1620031	Res network 0w06 2x1k0 j	0404	0404
R128	1430718	Chip resistor	47	5 % 0.063 W 0402
R131	1422881	Chip resistor	0.22	5 % 1 W 1218
R136	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R140	1430690	Chip jumper		0402
R142	1430690	Chip jumper		0402
R152	1430690	Chip jumper		0402
R154	1430122	Chip resistor	4.7 M	5 % 0.063 W 0603
R201	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R202	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R203	1620029	Res network 0w06 2x4k7 j	0404	0404
R211	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R213	1430690	Chip jumper		0402
R215	1620023	Res network 0w06 2x47k j	0404	0404
R252	1430740	Chip resistor	330	5 % 0.063 W 0402
R254	1620027	Res network 0w06 2x47r j	0404	0404
R256	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R257	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R259	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R260	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R261	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R263	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R265	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R267	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R268	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R270	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R271	1430804	Chip resistor	100 k	5 % 0.063 W 0402
R281	1430792	Chip resistor	33 k	5 % 0.063 W 0402
R282	1430798	Chip resistor	56 k	5 % 0.063 W 0402
R301	1620031	Res network 0w06 2x1k0 j	0404	0404
R303	1620031	Res network 0w06 2x1k0 j	0404	0404
R305	1620031	Res network 0w06 2x1k0 j	0404	0404

System Module

Technical Documentation

R307	1620031	Res network 0w06 2x1k0 j	0404	0404
R308	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R309	1620031	Res network 0w06 2x1k0 j	0404	0404
R401	1430778	Chip resistor	10 k	5 % 0.063 W 0402
R402	1430754	Chip resistor	1.0 k	5 % 0.063 W 0402
R403	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R404	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R405	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R406	1430693	Chip resistor	5.6	5 % 0.063 W 0402
R500	1430700	Chip resistor	10	5 % 0.063 W 0402
R501	1430700	Chip resistor	10	5 % 0.063 W 0402
R502	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R504	1620019	Res network 0w06 2x10k j	0404	0404
R507	1430740	Chip resistor	330	5 % 0.063 W 0402
R530	1430700	Chip resistor	10	5 % 0.063 W 0402
R531	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R533	1430796	Chip resistor	47 k	5 % 0.063 W 0402
R550	1430752	Chip resistor	820	5 % 0.063 W 0402
R551	1430740	Chip resistor	330	5 % 0.063 W 0402
R552	1430740	Chip resistor	330	5 % 0.063 W 0402
R553	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R554	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R555	1430726	Chip resistor	100	5 % 0.063 W 0402
R580	1430706	Chip resistor	15	5 % 0.063 W 0402
R581	1430832	Chip resistor	2.7 k	5 % 0.063 W 0402
R582	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R584	1430780	Chip resistor	12 k	5 % 0.063 W 0402
R585	1430774	Chip resistor	6.8 k	5 % 0.063 W 0402
R586	1430738	Chip resistor	270	5 % 0.063 W 0402
R588	1430744	Chip resistor	470	5 % 0.063 W 0402
R589	1430710	Chip resistor	22	5 % 0.063 W 0402
R600	1430788	Chip resistor	22 k	5 % 0.063 W 0402
R620	1620029	Res network 0w06 2x4k7 j	0404	0404
R621	1430744	Chip resistor	470	5 % 0.063 W 0402
R622	1430758	Chip resistor	1.5 k	5 % 0.063 W 0402
R623	1430714	Chip resistor	33	5 % 0.063 W 0402
R624	1430714	Chip resistor	33	5 % 0.063 W 0402
R625	1430714	Chip resistor	33	5 % 0.063 W 0402
R626	1430740	Chip resistor	330	5 % 0.063 W 0402
R627	1430776	Chip resistor	8.2 k	5 % 0.063 W 0402
R628	1430744	Chip resistor	470	5 % 0.063 W 0402
R629	1430730	Chip resistor	150	5 % 0.063 W 0402
R630	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R631	1430700	Chip resistor	10	5 % 0.063 W 0402
R632	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R634	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R635	1430851	Chip resistor	15 k	2 % 0.063 W 0402

R636	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R638	1430848	Chip resistor	12 k	1 % 0.063 W 0402
R640	1430734	Chip resistor	220	5 % 0.063 W 0402
R641	1820031	NTC resistor	330	10 % 0.12 W 0805
R660	1430726	Chip resistor	100	5 % 0.063 W 0402
R662	1430714	Chip resistor	33	5 % 0.063 W 0402
R664	1430764	Chip resistor	3.3 k	5 % 0.063 W 0402
R666	1430770	Chip resistor	4.7 k	5 % 0.063 W 0402
R668	1430732	Chip resistor	180	5 % 0.063 W 0402
R670	1430726	Chip resistor	100	5 % 0.063 W 0402
R706	1430812	Chip resistor	220 k	5 % 0.063 W 0402
R708	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
R710	1430762	Chip resistor	2.2 k	5 % 0.063 W 0402
C100	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C101	2320548	Ceramic cap.	33 p	5 % 50 V 0402
C102	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C103	2604127	Tantalum cap.	1.0 u	20 % 35 V 3.5x2.8x1.9
C104	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C105	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C106	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C107	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C108	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C109	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C110	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C112	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C113	2320508	Ceramic cap.	1.0 p	0.25 % 50 V 0402
C114	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C115	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C116	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C117	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C118	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C119	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C120	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C121	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C122	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C127	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C128	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C129	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C130	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C131	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C132	2312403	Ceramic cap.	2.2 u	10 % 10 V 1206
C133	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C140	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C141	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C142	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C143	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C160	2320546	Ceramic cap.	27 p	5 % 50 V 0402

System Module

Technical Documentation

C161	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C201	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C202	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C203	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C204	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C205	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C206	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C207	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C208	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C209	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C211	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C212	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C213	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C221	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C231	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C247	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C248	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C249	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C251	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C252	2312296	Ceramic cap.		Y5 V 1210
C253	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C254	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C255	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C256	2312296	Ceramic cap.		Y5 V 1210
C257	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C258	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C260	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C261	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C262	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C263	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C266	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C268	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C269	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C271	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C272	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C301	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C302	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C303	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C304	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C305	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C306	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C307	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C308	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C309	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C310	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C311	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C312	2320546	Ceramic cap.	27 p	5 % 50 V 0402

C313	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C400	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C401	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C402	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C403	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C404	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C405	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C500	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C501	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C502	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C504	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C505	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C506	2320544	Ceramic cap.	22 p	5 % 50 V 0402
C507	2320550	Ceramic cap.	39 p	5 % 50 V 0402
C511	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C512	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C513	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C514	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C515	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C516	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C518	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C520	2320602	Ceramic cap.	4.7 p	0.25 % 50 V 0402
C530	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C531	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C532	2320554	Ceramic cap.	56 p	5 % 50 V 0402
C535	2310181	Ceramic cap.	1.5 n	5 % 50 V 1206
C540	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C550	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C553	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C554	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C555	2320618	Ceramic cap.	4.7 n	5 % 25 V 0402
C559	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C562	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C563	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C564	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C565	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C566	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C567	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C568	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C570	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C571	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C572	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C574	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C575	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C576	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C582	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C583	2320544	Ceramic cap.	22 p	5 % 50 V 0402

System Module

Technical Documentation

C585	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C586	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C587	2310248	Ceramic cap.	4.7 n	5 % 50 V 1206
C588	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C590	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C592	2610003	Tantalum cap.	10 u	20 % 10 V 3.2x1.6x1.6
C600	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C601	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C602	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C603	2320584	Ceramic cap.	1.0 n	5 % 50 V 0402
C604	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C610	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C611	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C612	2610013	Tantalum cap.	220 u	10 % 10 V 7.3x4.3x4.1
C613	2320538	Ceramic cap.	12 p	5 % 50 V 0402
C614	2320526	Ceramic cap.	3.9 p	0.25 % 50 V 0402
C621	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C622	2320514	Ceramic cap.	1.2 p	0.25 % 50 V 0402
C623	2320534	Ceramic cap.	8.2 p	0.25 % 50 V 0402
C624	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C627	2320738	Ceramic cap.	470 p	10 % 50 V 0402
C630	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C632	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C633	2320532	Ceramic cap.	6.8 p	0.25 % 50 V 0402
C635	2320560	Ceramic cap.	100 p	5 % 50 V 0402
C636	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C638	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C639	2320592	Ceramic cap.	2.2 n	5 % 50 V 0402
C640	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C641	2310784	Ceramic cap.	100 n	10 % 25 V 0805
C642	2320552	Ceramic cap.	47 p	5 % 50 V 0402
C643	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C644	2320540	Ceramic cap.	15 p	5 % 50 V 0402
C649	2320131	Ceramic cap.	33 n	10 % 16 V 0603
C652	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C653	2320536	Ceramic cap.	10 p	5 % 50 V 0402
C655	2320530	Ceramic cap.	5.6 p	0.25 % 50 V 0402
C656	2320620	Ceramic cap.	10 n	5 % 16 V 0402
C660	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C662	2320546	Ceramic cap.	27 p	5 % 50 V 0402
C695	2312401	Ceramic cap.	1.0 u	10 % 10 V 0805
C700	2320524	Ceramic cap.	3.3 p	0.25 % 50 V 0402
L103	3203701	Ferrite bead 33r/100mhz	0805	0805
L104	3203701	Ferrite bead 33r/100mhz	0805	0805
L105	3203701	Ferrite bead 33r/100mhz	0805	0805
L106	3640035	Filt z>450r/100m 0r7max 0.2a	0603	0603
L107	3640035	Filt z>450r/100m 0r7max 0.2a	0603	0603

Technical Documentation

System Module

L108	3640035	Filt z>450r/100m Or7max 0.2a 0603	0603
L400	3640035	Filt z>450r/100m Or7max 0.2a 0603	0603
L500	3643039	Chip coil	220 n
L501	3643039	Chip coil	220 n
L550	3640069	Filt 47pf 25v Or01 6a 1206	
L552	3645157	Chip coil	100 n
L554	3645157	Chip coil	100 n
L580	3645161	Chip coil	150 n
L581	3643025	Chip coil	56 n
L600	3641206	Chip coil	
L621	3641300	Chip coil	330 n
L623	3641626	Chip coil	220 n
L624	3641626	Chip coil	220 n
B100	4510003	Crystal	32.768 k
G530	4350099	Vco 1006-1031mhz 2.8v 10ma gsm	
G600	4510153	VCTCXO	13.0 M
F101	5119019	SM, fuse f 1.5a 32v 0603	
Z500	4511017	Saw filter	947.5+-12.5 M
Z505	4511015	Saw filter	902.5+-12.5 M
Z550	4512005	Dupl 890-915/935-960mhz 20x14	20x14
Z620	4510009	Cer.filt 13+-0.09mhz 7.2x3.2	7.2x3.2
Z621	4510137	Saw filter	71+-0.09 M
V100	1825005	Chip varistor vwm14v vc30v 0805	0805
V101	4113651	Trans. supr.	QUAD
V102	4113651	Trans. supr.	QUAD
V103	4113601	Emi filter emif01-5250sc5 sot23-5	SOT23-5
V104	4113651	Trans. supr.	QUAD
V116	4110067	Schottky diode	MBR0520L
V250	4210100	Transistor	BC848W
V550	4110014	Sch. diode x 2	BAS70-07
V580	4110062	Cap. diode	BB535
V581	4210066	Transistor	BFR93AW
V640	4210066	Transistor	BFR93AW
V705	4210100	Transistor	BC848W
D200	4370279	Mad2 rom3 f711604 c12 tqfp176	TQFP176
D211	4340261	Te28f800 flashm 512kx16 120ns	
D220	4340273	IC, SRAM	STSOP32
D230	4342264	IC, EEPROM	SO8S
D402	4340369	IC, dual bus buffer sso TC7W126FU	SSOP8
N100	4370047	Ccont 2f dct3 bb asic tqfp64	TQFP64
N101	4370165	Uba2006t chaps charg.control so16	SO16
N201	4340423	IC, regulator	TK11230M
N250	4370317	Cobba_gj b07 bb asic dct3 tqfp64	TQFP64
N400	4860031	Tfdu4100 irda tx/rx>2.7v 115kbits	115KBITS
N500	4370253	Crfu1a rx+tx uhf gsm v5 sot401-1	SOT401-1
N550	4370319	Rf9106 pw amp 880-915mhz psop2-16	PSOP2-16

N620	4370273	Plussa txmod+rxif+2pll	tqfp64	TQFP64	
S301	5219005	IC, SWsp-no 30vdc 50ma	smSW TACT		SMD
S302	5219005	IC, SWsp-no 30vdc 50ma	smSW TACT		SMD
X100	5469061	SM, system conn 6af+3dc+mic+jack			
X101	5469069	SM, batt conn 2pol spr p3.5	100v	100V2A	
X102	5469069	SM, batt conn 2pol spr p3.5	100v	100V2A	
X300	5460021	SM, conn 2x14m spring p1.0	pcb/p	PCB/PCB	
X302	5400085	Sim card reader 2x3pol p2.54	sm	SM	
X540	5429007	SM, coax conn m sw 50r 0.4-2ghz			
A500	9517012	SM, d rf shield dmc00422	hd940 u	UP8	
A510	9517013	SM, d rf shield pa-can dmc00455			
	9380753	Bar code label dmd03311	27x6.5	27x6.5	
	9850051	PCB UP8 123.25X41.0X1.0	M6 4/PA		
	9850051	PC board	UP8	123.25x41.0x1.0	m6 4/pa

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